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VOICE OF THE ENGINEER

NOV 8

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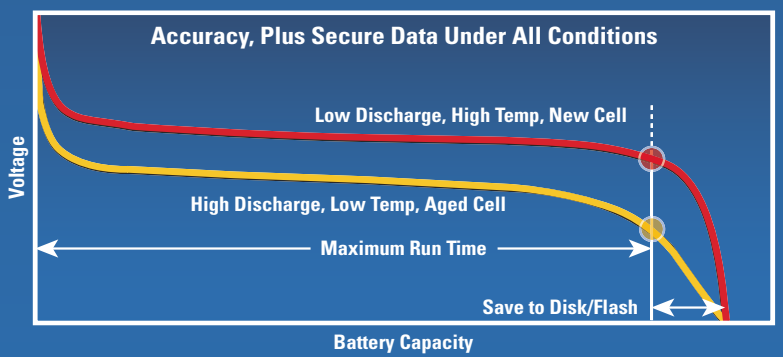

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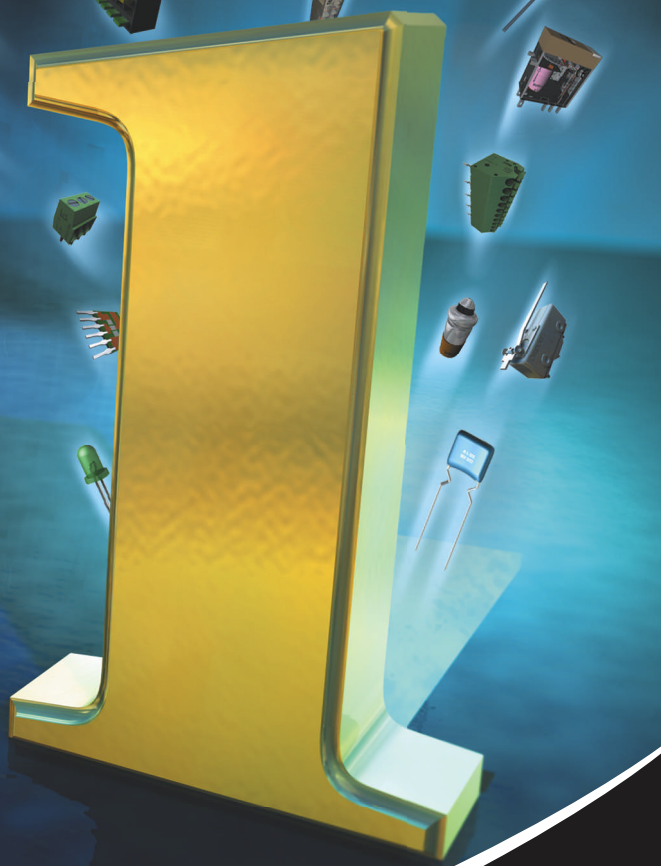

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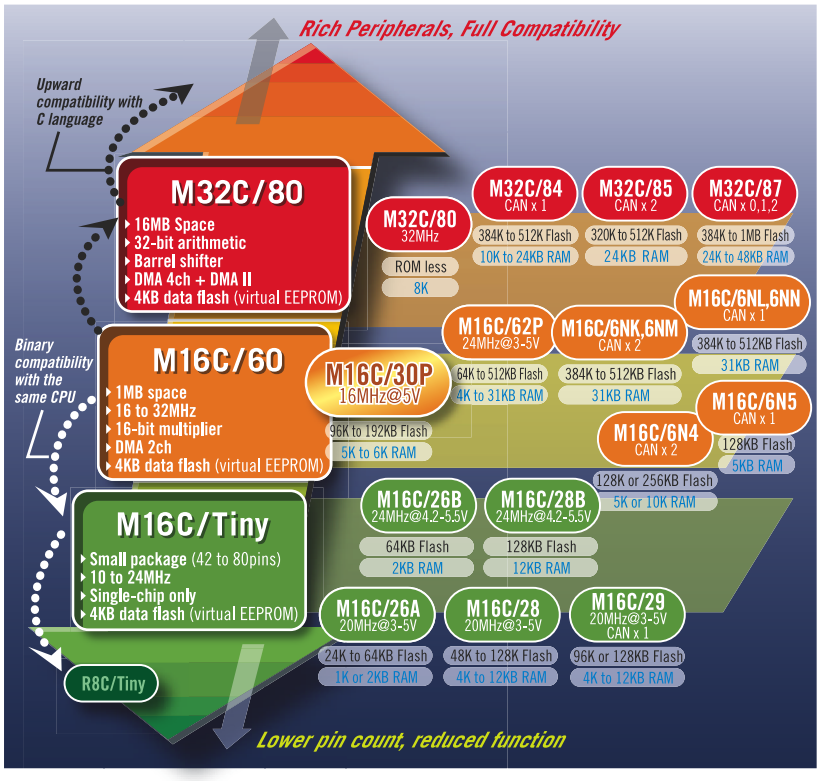
M16C Product Lineup

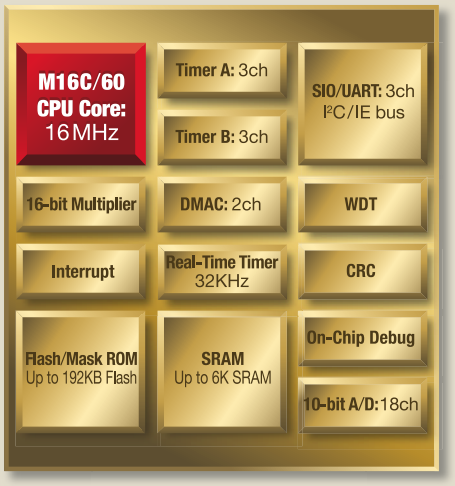


HOT Products | **M16C/30P Group**

3 cents per pin*

* M30302FCPGP#U5C 100 pin LQFP 128K Flash /5K RAM

M16C/30P Block Diagram



Top Reasons to select M16C MCU

- **Broad Platform & Compatibility**
  - Wide selection; 24KB to 1MB Flash, 42 to 144 pin
  - Up/downgrade in same package, same board design
  - Saves costs and protecting code investment.
- **Powerful and Easy**
  - Banked registers & high speed interrupts (M32C)
  - Optimized instructions for 1cycle operations
  - High-speed hardware multiplier
  - Common Tool Chain across the platform
  - Proven middleware; ZigBee, CAN, motor control
- **Versatile & Efficient**
  - Specialized peripherals; CAN, PLC, motor control
  - Efficient mapping for practical application
  - Flexible DMAC for efficient connectivity
  - Multiple clock sources and power saving modes
- **Quiet EMI/EMS**
  - Built-in noise cancellation, fewer components
- **Reliable and Secured**
  - Trusted flash and protection registers
  - Fail-safe features; oscillator-stop, non-stop WDT.

Source: Gartner (March 2007) "2006 Worldwide Microcontroller Vendor Revenue" GJ07168

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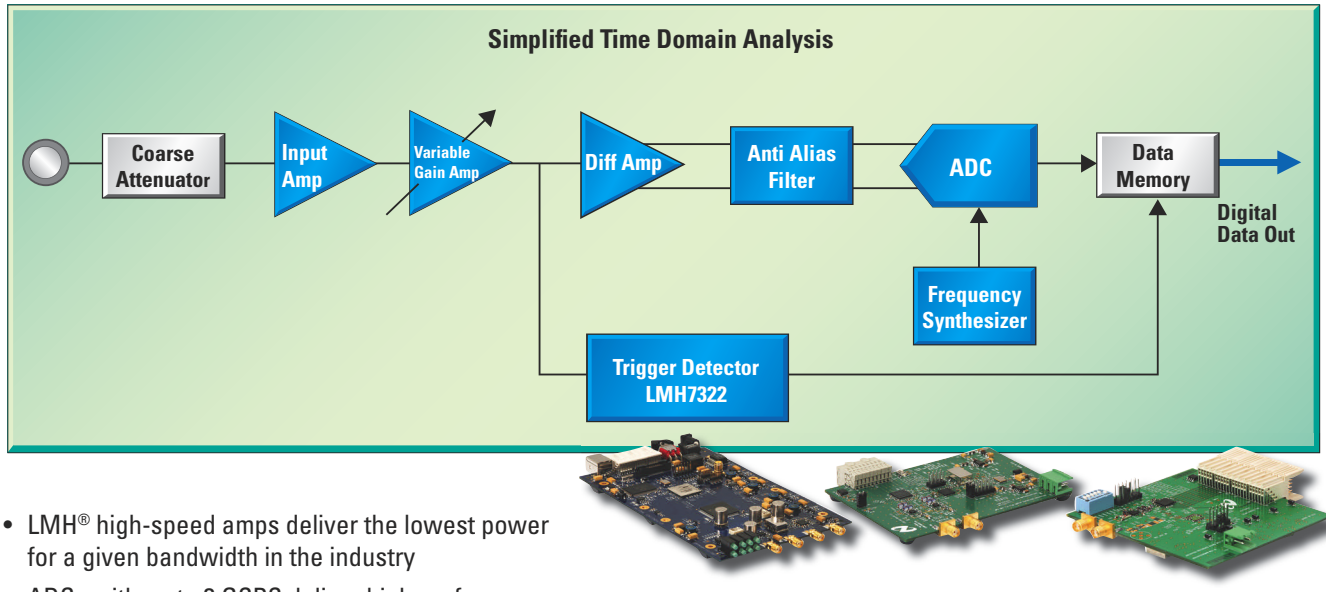

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- ADCs with up to 3 GSPS deliver high performance at the lowest power consumption
- Programmable precision clock conditioners featuring jitter performance as low as 0.2 ps

Analog to Digital Converters

Product ID	Description
ADC083000/B3000	8-bit, 3 GSPS / 3 GSPS with capture buffer
ADC14155/V155	14-bit, 155 MSPS, CMOS or LVDS outputs
ADC14DS105	14-bit, 105 MSPS, serial LVDS outputs

Differential Amplifiers

Product ID	Description	Bandwidth	Noise Figure	Linearity	Packaging
LMH6515	Digitally controlled variable gain amplifier, 31 dB gain range	600 MHz	8.3 dB	40 dBm OIP3	LLP-16
LMH6552	Fully differential amplifier	1.5 GHz	10.3 dB	35.5 dBm OIP3	LLP-8, SOIC-8
LMH6555	Differential fixed gain amplifier	1.2 GHz	15 dB	-50.5 dBc THD at 750 MHz	LLP-16

Clock Conditioners

Product ID	Description	LVDS Outputs	LVPECL Outputs	VCO	PLL	Jitter (RMS) (typ)
LMK02000	Clock conditioner	3	5	—	Integrated	20 fs
LMK03000	Clock conditioner	3	5	Integrated	Integrated	400 fs
LMX2531	Frequency synthesizer	1	—	Integrated	Integrated	400 fs

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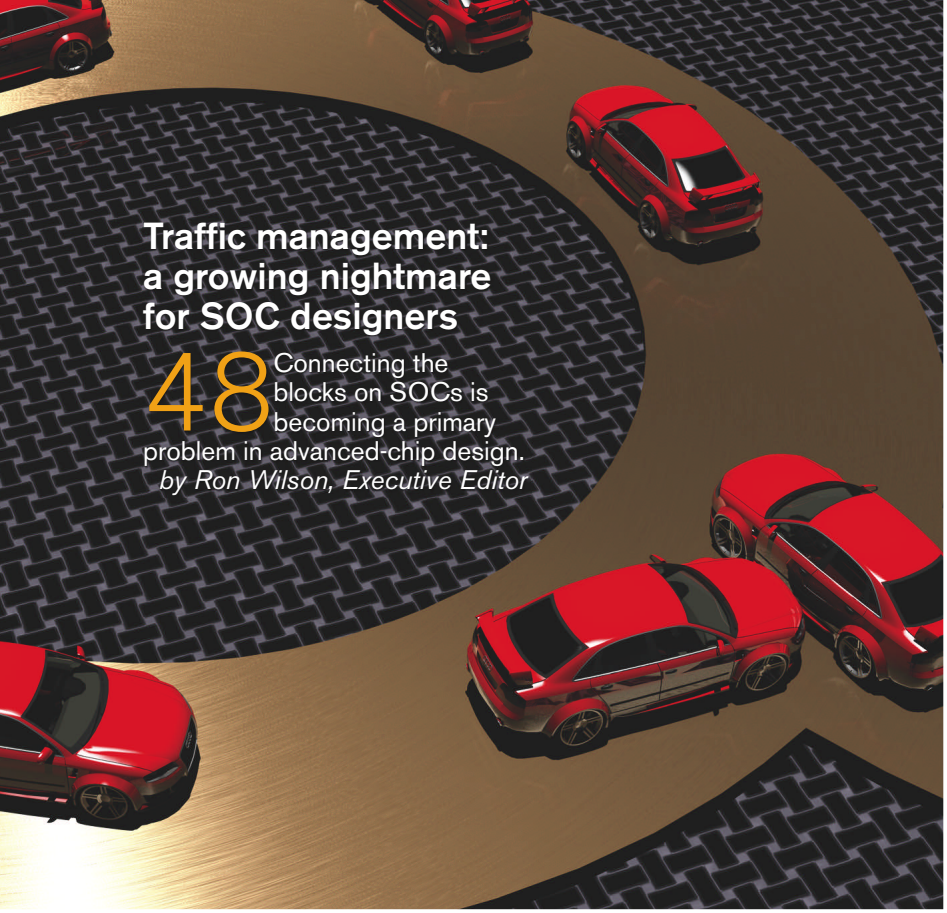
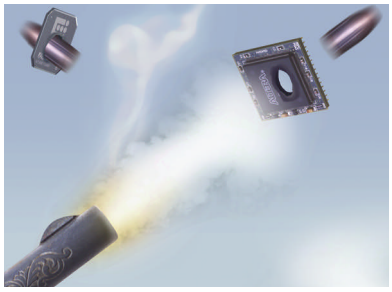
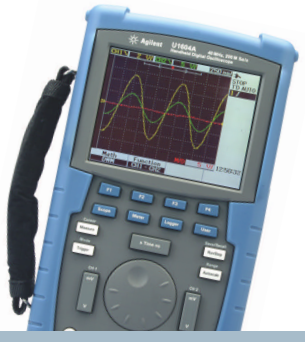


Traffic management: a growing nightmare for SOC designers



High noon for FPGAs: low-cost-versus-high-end showdown

Handheld oscilloscopes offer varied features

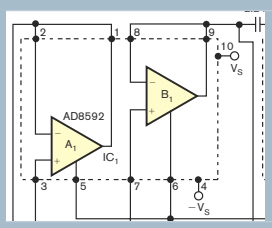


59 GLOBAL REPORT

Globally, engineers share similar gratification and concern

Reference designs worldwide: understanding the IP imbalance

DESIGNIDEAS



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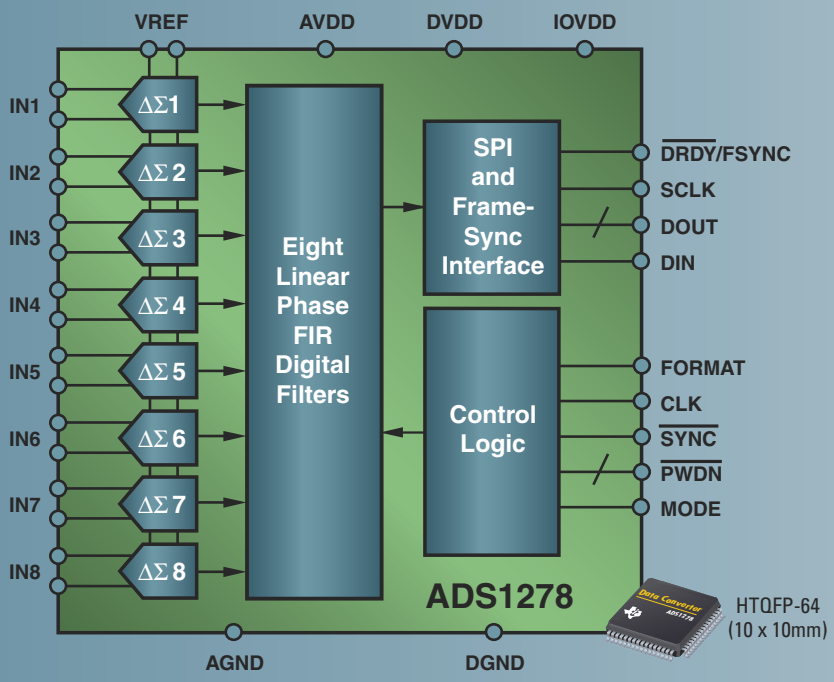
4- and 8-Channel, 128kSPS, Industrial ADCs



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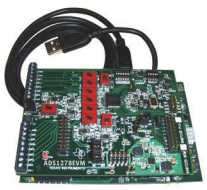
ADS1178	16-bit	8	97dB	±0.0008	$15.95
ADS1174	16-bit	4	97dB	±0.0008	$9.95

** Suggested resale price in U.S. dollars in quantities of 1,000.*



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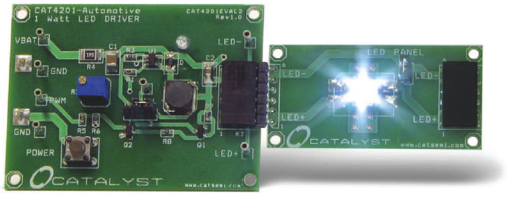

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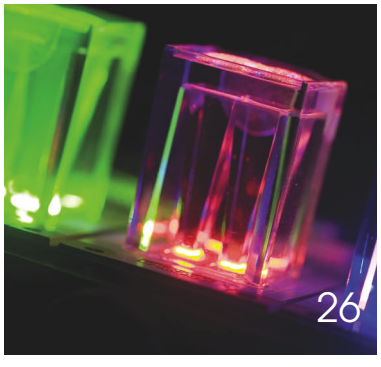

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DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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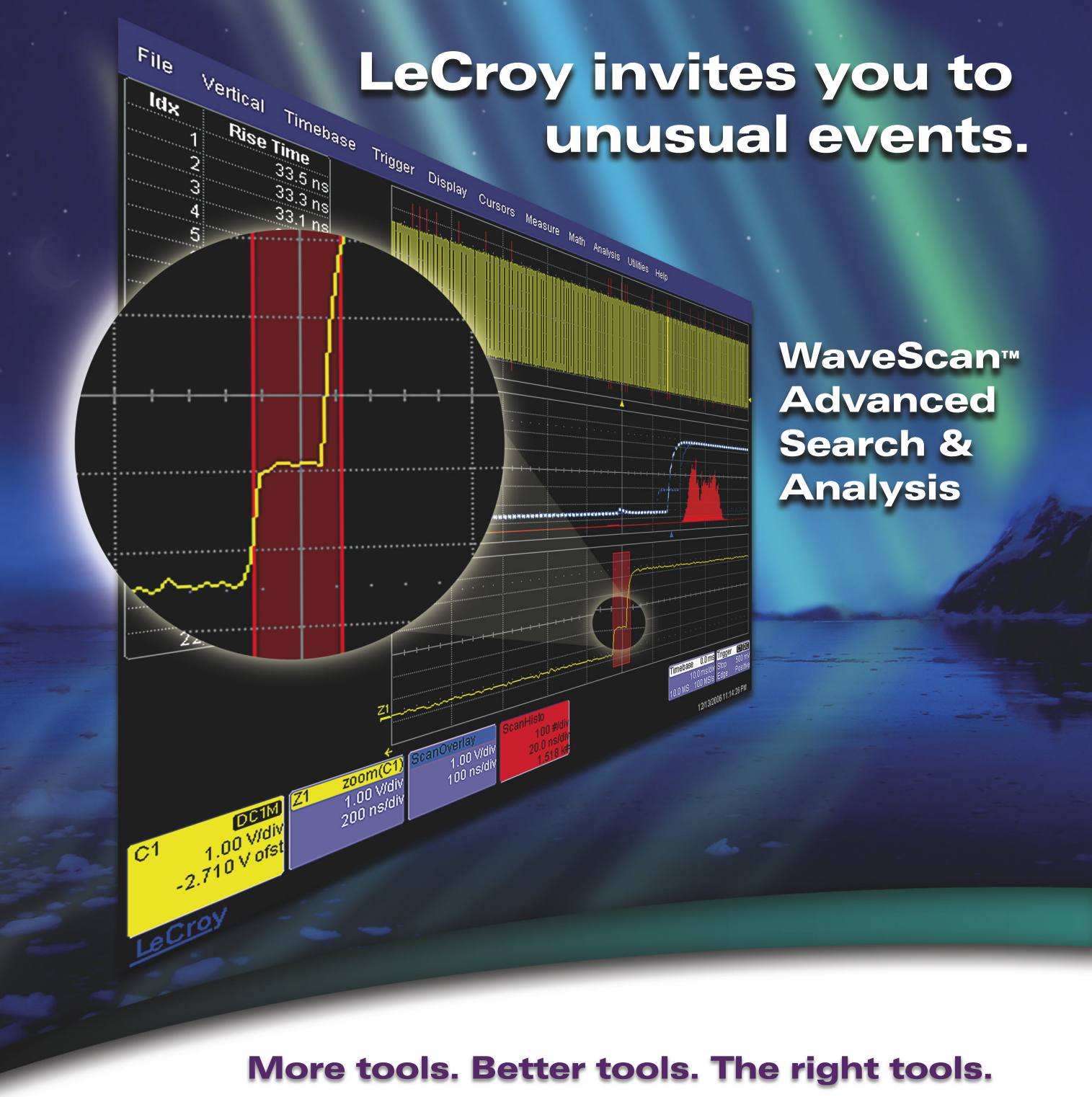

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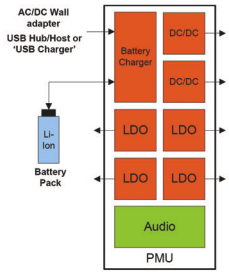

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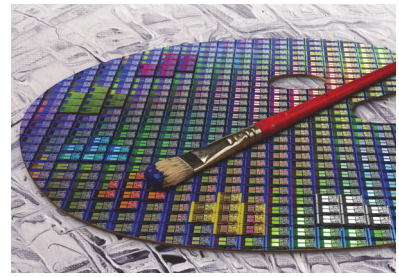

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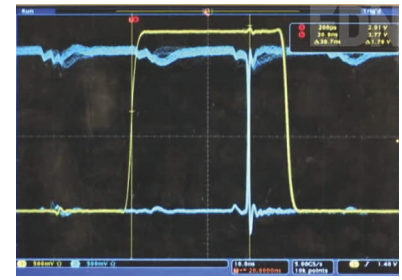

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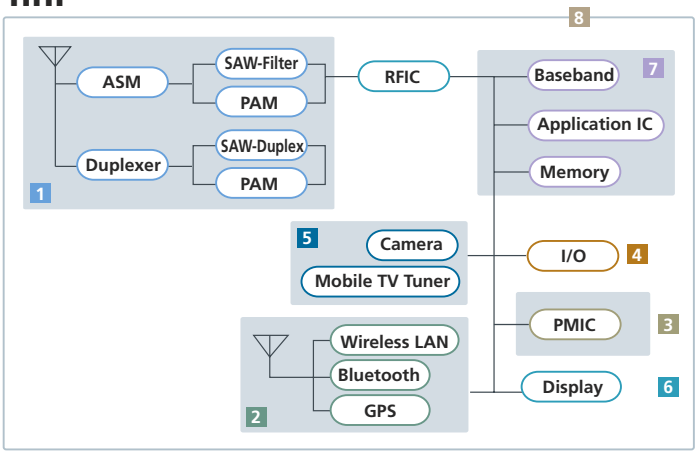

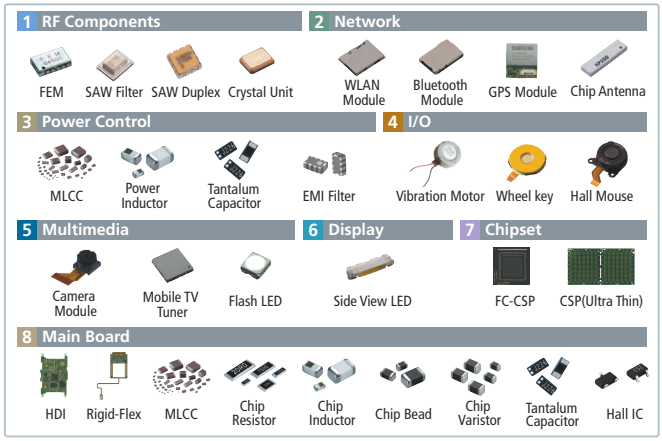

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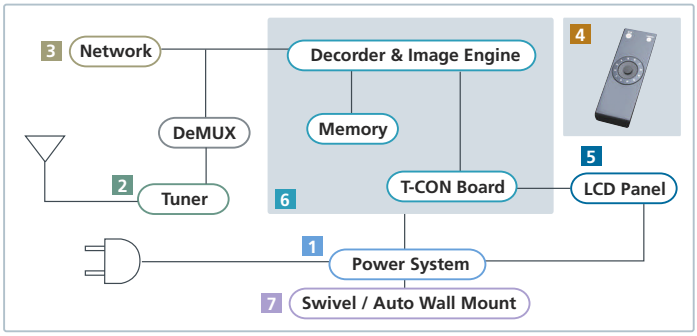
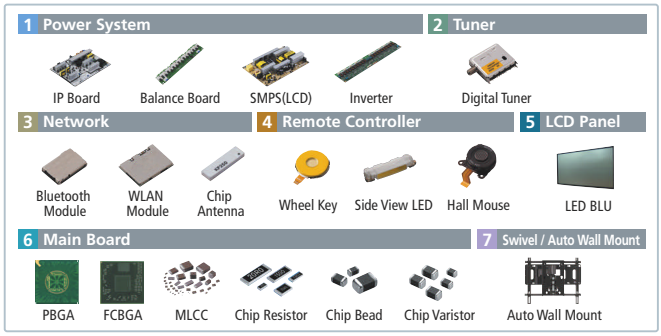
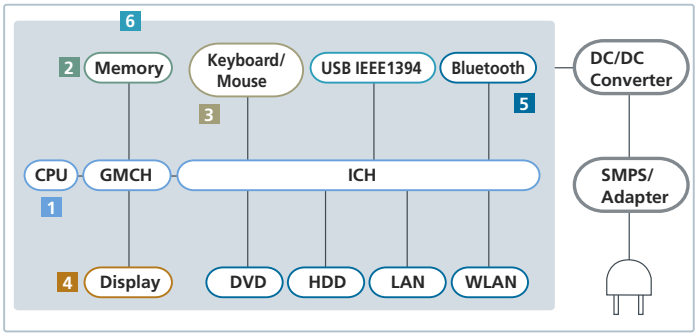
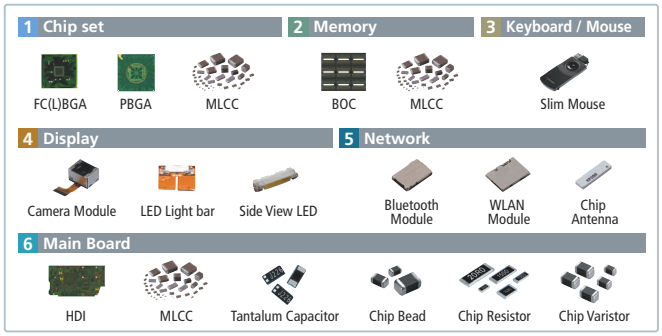




PC





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BY MAURY WRIGHT, EDITORIAL DIRECTOR

Global Report highlights careers and reference designs

Once a year, *EDN* marshals its resources across Asia, Europe, and North America to produce a *Global Report* that we present in every edition of *EDN* worldwide. In the past, we've focused on global standards and regulatory issues, enabling technologies that matter on a global basis, and the applications driving the global-technology economy. This year, we change things up and look at the electronics-engineering profession. We also take a look at the phenomenon of reference designs, because these designs play differing roles in the the daily work life of engineers around the world. This year's *Global Report* starts on page 59, and, as always, you'll find additional articles online at www.edn.com/global.

As the basis for the career portion of the *Global Report*, we fielded a global salary and career-satisfaction survey. We found that engineers worldwide cherish the creative and innovative aspects of their jobs, but they also share concerns about job security and long work hours. Not surprisingly, engineers in the mature electronic markets of Europe, Japan, and North America enjoy far larger salaries than their counterparts in developing regions. But almost all engineers share the feeling that they are underpaid and even underappreciated. Still, in a strange conundrum, most engineers are content with their career choice.

The aspirations of engineers globally provide an interesting contrast. Design engineers in Korea would like to stay on a technical-career track, yet their employers often force them into managerial roles. In China, conversely, engineers feel that, to succeed, they must move into sales, marketing, or management by the age of 35.

The second article in the *Global Report* examines the increasingly important role that reference designs now play in design. Reference designs help engineers get increasingly complex products to market on time and are invaluable for IC and component vendors. A comprehensive reference design can be the prime factor for a maker of an application-specific SOC (system on chip) in getting that IC adopted. However, even vendors of secondary components win by having a reference design include their components.

Nevertheless, designers in different regions look for different features in reference designs. Check out Contributing Technical Editor Nicholas Cravotta's "Reference designs worldwide: understanding the IP imbalance," which begins on pg 75, for a generalized look at the phenomenon. Then, peruse the **sidebars** by *EDN* editors around the globe for firsthand accounts from engineers in each region of the relevance of reference designs and how designers use them.

With the release of the 2007 *Global Report*, we also present the online results of our North American salary and career-satisfaction survey. You'll find links to that data from the online version of the *Global Report*. We also present portions of the surveys from *EDN* editions in Asia and Europe.

As always, I appreciate your feedback. Let me know what you think about the *Global Report*. Digest the contents of our salary and career-satisfaction survey and respond with your own thoughts. You can contact me directly by phone or e-mail. But, if you respond in the Feedback Loop you'll find alongside the online version of the article of interest, your fellow engineers will be able to access your thoughts and share theirs. EDN

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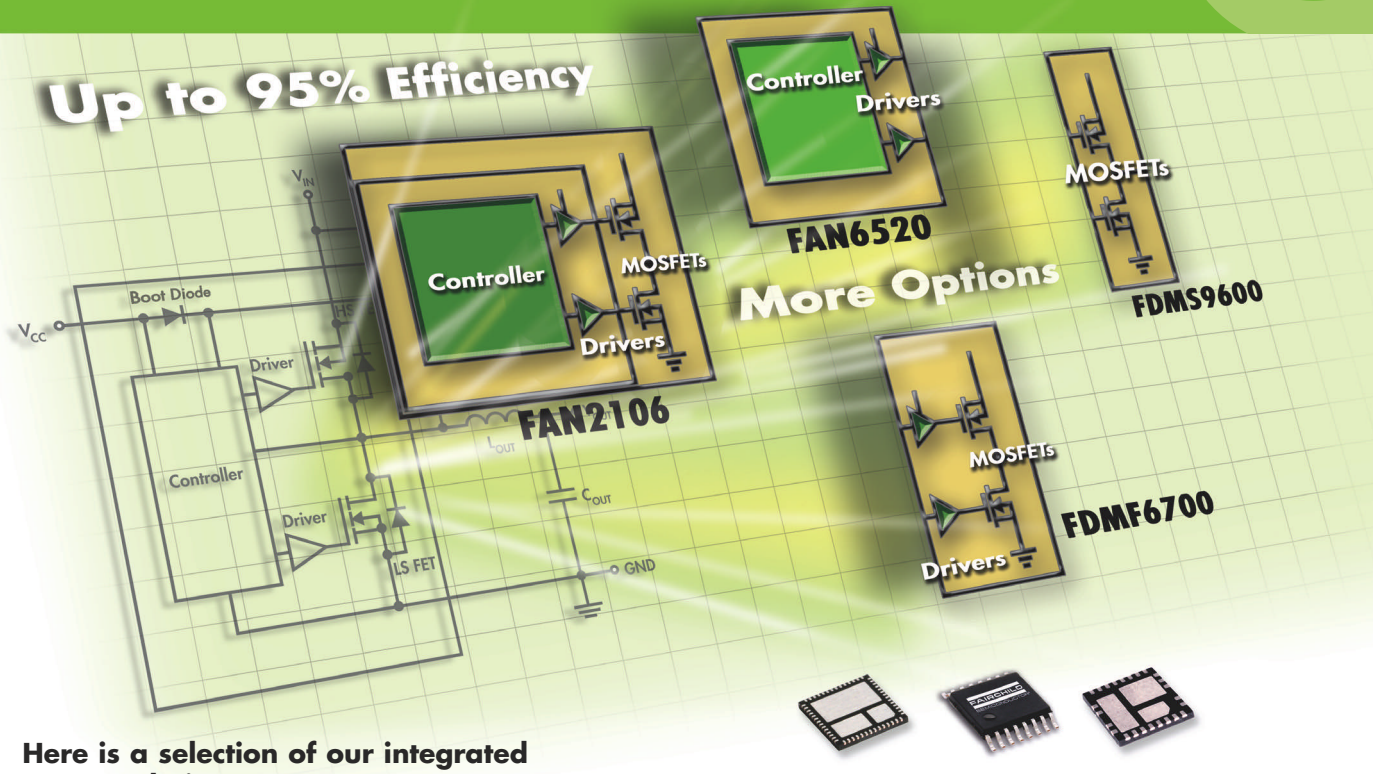

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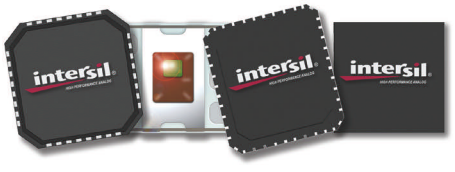

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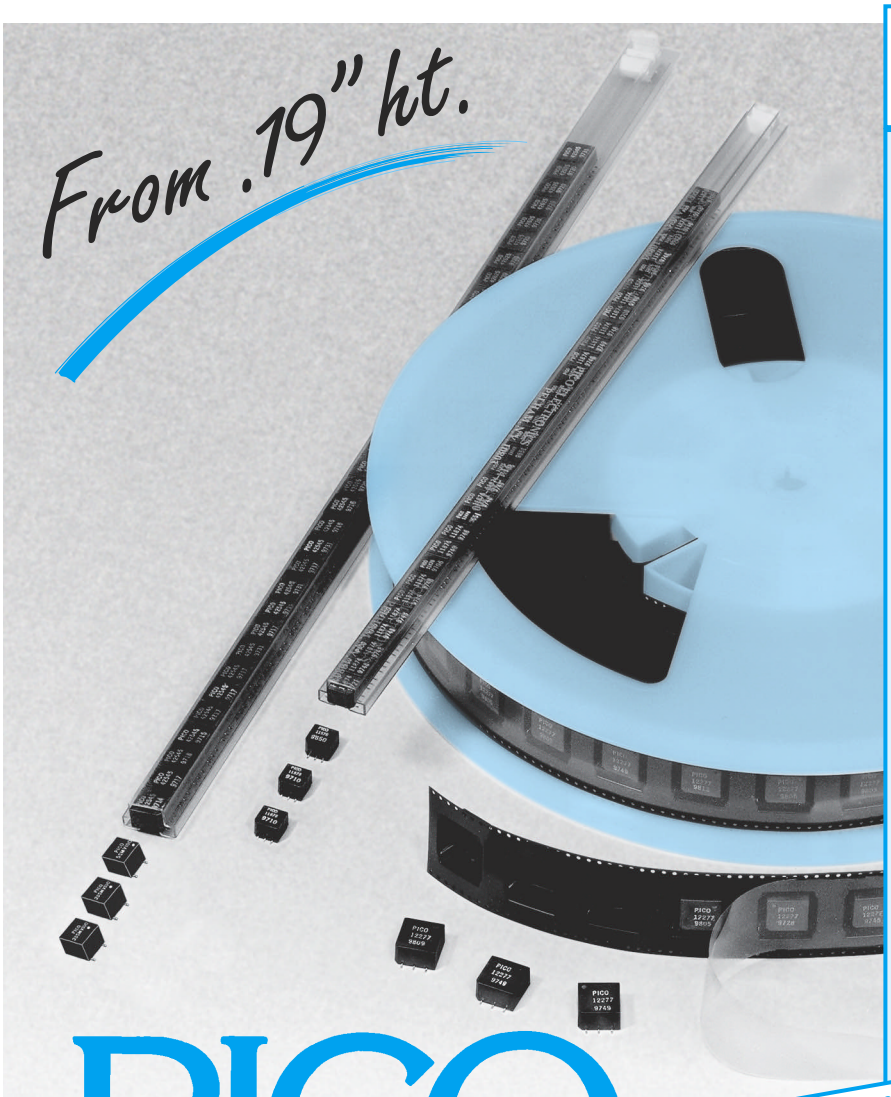

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Dealing with EMI in Class D Audio Applications

Application Note AN-1737

Bill McCulley, Applications Engineer

EMI – The Basics

Electromagnetic Interference (EMI) is an unwanted disturbance caused in an electrical circuit by electromagnetic radiation emitted from an external source. EMI encompasses two aspects. Emissions refer to the scope to which equipment generates radiated noise. Susceptibility is the scope to which equipment is affected by emissions generated from other electromagnetic waves. The degree to which the designer controls unintended emissions may make the task of susceptibility easier. In order to understand emissions, it is important to understand antennas. ***Figure 1*** below shows the well-known physical relationship between wavelength and frequency:

$$\lambda = \frac{Velocity\ \ of\ \ Light}{Frequency \times \sqrt{\epsilon_r}} = \frac{300}{f\,(MHz) \times \sqrt{\epsilon_r}}$$

ϵ_r is the relative permittivity

Figure 1. Wavelength as a Function of Frequency

The shortest length required to be an efficient antenna is λ/4. In the case of air, permittivity is 1, but in the case of FR4 or glass-epoxy PCBs, permittivity is reduced to approximately 4.8. The effect causes a signal traveling a trace to slow once it reaches the dielectric gradient created by the FR4 material, causing essentially, a "wavelength-shortening" effect. For example:

A 200 MHz signal has a quarter wavelength in air of 16.7 cm.

In an inner-layer PCB trace, it is: $16.7/4.8^{(1/2)} = 7.6$ cm.

A PCB trace can act as an unintentional antenna even at lengths shorter than λ/4, increasing both emissions and susceptibility. Surface traces also exhibit this wavelength-shortening effect, as one side of the dielectric serves to change the overall permittivity of the transmission.

Unintended antennas, such as PCB traces, are the key culprit behind radiated noise in digital systems. As we will see, the Class D audio amplifier is, in essence, a digital system from the perspective of radiated emissions. Unintended antennas in circuit boards can include long traces, vias, leads, and unpopulated PCB connectors or headers.

The Class D Audio Amplifier

The Class D audio amplifier has emerged as a popular topology for the consumer market due to its high efficiency. It modulates a high-frequency square wave by the incoming analog signal. A low-pass filter, typically a 2-pole Butterworth, is used to filter the high-frequency content and recover the original audio signal. In "filterless" topologies, the inductance of the speaker itself is incorporated as part of the filter. One common Class D topology, Pulse Width Modulation (PWM), uses a fixed-frequency waveform and changes the duty cycle to create a moving average of the signal after a low-pass filter, as seen in ***Figure 2.***

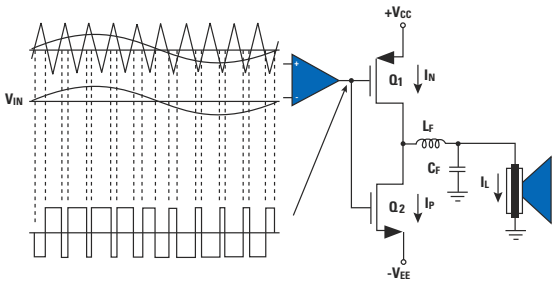

Figure 2. The Class D Audio Amplifier PWM

The benefits of a switching topology are apparent – high efficiency, low-power consumption, and small thermal designs. But increased efficiency is not without cost. In order to drive efficiencies up, a sharp rapidly-switching square wave is required. This can lead to the same undesirable artifacts that are present in digital systems, as the spectral energy is highly concentrated on the edges of the square wave.

Countering EMI

To counter EMI, it is essential to include PCB floor planning as part of the circuit design. General PCB guidelines for dealing with EMI include:

- Appropriate placement of decoupling capacitors between power and ground
- Avoidance of traces cut within ground or power planes
- Adequate termination of all high-frequency clock lines
- Proper filtering of PCB connectors
- Avoid loop antennas

Optimally, you will stop radiation by suppressing the source of current that is feeding the antenna.

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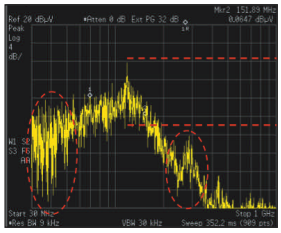
For the audio designer, it is important to consider the following:

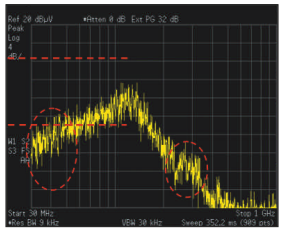
- Keep traces from the audio amplifier to the speaker as short as possible. Traces and wires act as antennas with significant radiation occurring once the length reaches λ/4
- For filterless Class D systems, the trace and wire connecting the amplifier's output to the speakers will likely be the largest source of emissions

The practice of placing ferrite beads in series with the loudspeakers close to the amplifier can be effective. Regarding EMI suppression purposes, ferrite beads act as resistors, but because R_{DC} = 0, there is no DC voltage drop. This makes them useful in cases where frequencies of interest are significantly below 1 MHz. Also, it is important to under- stand that the ferrite bead is effective when considered part of a two-element voltage divider. The ferrite will usually serve as the series element, and the shunt element is a capacitance – either a physical capacitance or a lumped capacitance. The transfer function indicates the system will be damped to the extent that resonance effects are significantly diminished.

The primary difficulty with periodic square waves inherent in Class D is the concentration of energy at the harmonic intervals. In the push to create a "quiet" low-EMI Class D amplifier, one approach is to spread the spectrum of the switching so the energy at any one point in the spectrum is reduced. Efficiency and low THD+N are maintained, but radiated noise and EMI can be significantly reduced, as seen in ***Figure 3.***



Fixed-Frequency



Spread-Spectrum

Figure 3. Comparison of Fixed-Frequency and Spread-Spectrum Modulation

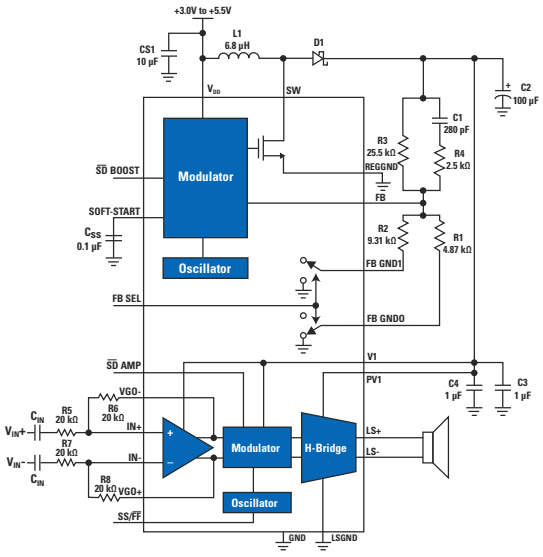


Figure 4. LM48511 – A Spread-Spectrum Modulated Class D Amplifier

The LM48511 is a spread-spectrum modulated Class D audio amplifier. It also includes a built-in boost regulator, which drives the supply voltage to 7V, increasing amplifier output power and the audio-sound pressure level compared to an unboosted amplifier. The boost regulator allows the amplifier to maintain a constant output level, even when powered from a decaying voltage source such as a battery.

The LM48511 amplifier features a logic-selectable, spread-spectrum modulator that reduces EMI, eliminating the need for output filters or chokes. As shown in ***Figure 4***, the spread-spectrum modulator feeds a standard H-bridge which drives the bridge-tied load speaker. In spread-spectrum mode, the switching frequency varies randomly by 10% around a 330 kHz center frequency, decreasing EMI emissions radiated by the speaker and associated cables and traces.

Electromagnetic interference is a system-level concern, and it is essential for today's audio engineer to design with EMI in mind, including the best possible design practices and judicious choice of components and materials.

For an expanded version of this article as well as additional reference information, please visit: edge.national.com ■

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pulse

INNOVATIONS & INNOVATORS

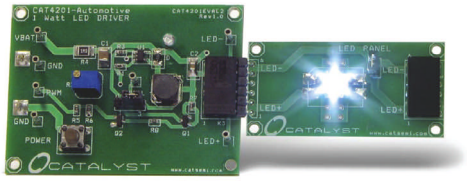
7W LED-driver IC provides 350 mA

Targeting use in tunnel-lighting, automotive-lighting, and similar applications, the new Catalyst Semiconductor CAT4201 buck-regulator driver can deliver 7W of power to a string of white LEDs operating from a 24V rail. The device delivers 1W when driving an LED off a 6V rail and delivers as much as 350 mA to the LED. By using a buck-regulator rather than a linear-regulator architecture, the device achieves efficiency as high as 94%. Catalyst manufactures the device using a high-performance, high-voltage CMOS process so that it can withstand 40V transients on the input. A single pin provides dimming and control.

A designer establishes the chip's switching frequency, which depends on the value of the inductor in the circuit rather than on the resistor-to-capacitor ratio. The device allows the inductor to run out of current, so it always operates just into the discontinuous mode. The peak current is twice the average current because the current goes to exactly 0A before the part turns on again. This feature allows a resistor that sets the peak current to also establish the average current. Using low-value inductors causes the operating current to rise and fall faster than it would with high-value inductors, resulting in a faster operating frequency for a given input voltage. Using this method, you can set the switching frequency at 50 kHz to 1 MHz.

In practice, an inductor value of 33 µH provides a 350-mA drive current across a wide range of input voltages. "The part detects when the inductor current goes to 0A and therefore can operate at the crossover point between continuous and discontinuous operation," says Anthony Russell, Catalyst's director of power-management products. "The frequency depends on the inductor value and the supply voltage." The CAT4201 is available in an ROHS (restriction-of-hazardous-substances) TSOT-23-5 package and sells for 72 cents (10,000). A demo board is available.**—by Paul Rako**

▷**Catalyst Semiconductor**, www.catsemi.com.



The CAT4201buck-LED-driver demo board and LED-module board target automotive applications.

FEEDBACK LOOP

"The pride in getting a design right the first time is worth the extra effort. There is no substitute for knowing that, and 'accurate' simulations will take as long as prototyping the real-deal PCB. ... The experience factor is missing from today's students who want to simulate everything. Life is not a video game that can be reset."

—Design engineer Kirk A Middlemass, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6475012. Add your comments.

Power supplies help PCs get their graphics game on

A standard desktop PC might come with a 300W power supply—more than adequate for most PC chores. But if you need to do serious graphics work that requires a graphics board, such as Nvidia's (www.nvidia.com) SLI 3D or ATI's (www.ati.com) Crossfire graphics-processor cards, your PC will need a bigger power supply. For those needs, you might consider Corsair's new TX Series of power supplies, available in the 650W CMPSU-650TX and the 750W CMPSU-750TX models. The supplies have dedicated single-12V-rail, active-PFC (power-factor-correction) circuitry, providing a PFC value of 0.99 under full load and 80% or greater energy efficiency across 20, 50, and 100% load conditions. The $179.99, 650W model includes two eight-pin (six-plus-two) PCIe (PCI Express) cables; the $199.99, 750W model has four PCIe cables.**—by Margery Conner**

▷**Corsair**, www.corsair.com.

The TX series of PC power supplies achieves greater than 80% power efficiency across its load range.

Start-up Solido optimizes transistor-level statistical analysis

With its new SolidoStat tool set, Solido Design Automation wants to help analog-system and full-custom-digital-system designers get more insight into the statistical-analysis step of the traditional tool flow. Statistical-timing analysis and Monte Carlo simulation are common steps in these tool flows, but most designers typically use a Monte Carlo simulation to determine parametric yield for their designs. After they run simulation, however, they don't know which parts of the design contribute to the statistical distribution for yield and how they can improve it without negatively impacting other parts of their design. A small change in a design can sometimes result in a big boost in performance. At other times, a small change can cause big problems for other parts of a design.

In standard digital design, designers encounter only a handful of design specifications and interdependence between variables, such as power, timing, yield, and signal integrity. Designers working at the transistor level, however, typically encounter hundreds or thousands of variables, according to Amit Gupta, Solido's co-founder and chief executive officer. Transistor-level designers typically must balance specifications, including gain, phase margin, slew rate, CMRR (common-mode-rejection ratio), power dissipation, offset voltage, offset current, bias current, and gain-bandwidth settling time, for each transistor. "You have to account for these [specs] simultaneously; you can increase your phase margin and worsen your gain or increase your gain and worsen your phase margin," says Gupta.

Environmental effects can also affect your design. "If you have voltage, temperature, and load conditions … for each of those [conditions], and all the variations, you have 27 combinations of environmental effects that you must consider simultaneously," he says. On top of these complications, designers must also account for global statistical variations, such as delta length and width; device variables, such as length and width; and local statistical variations, such as flatband voltage, N substrate, and mobility. "When you add all these effects simultaneously impacting your design, … there are literally thousands of variables that you must consider," Gupta says. To address these variables, designers typically design using worst-case scenarios. Doing so usually ensures that you hit yield margins but can also cause you to sacrifice performance, power savings, or other desirable effects.

> The tool employs parallel-processing and proprietary sampling algorithms to provide a speedup in Monte Carlo simulation.

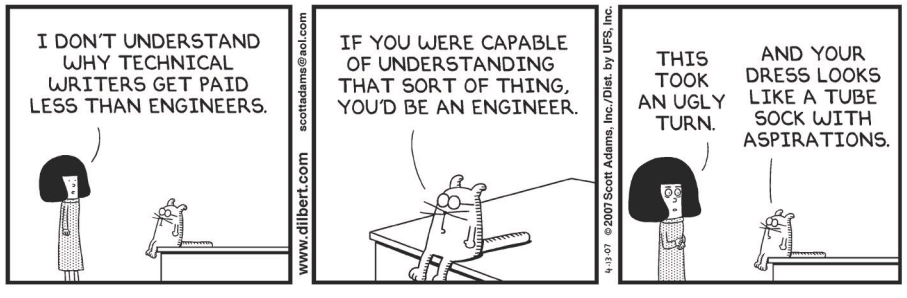
Solido believes it can help designs achieve greater performance, lower power, and yield targets with the SolidoStat tool suite, which includes Sampler, Characterizer, CircuitEnhancer, TradeoffAnalyzer, and Visualizer. The tools work with all large EDA vendors' SPICE simulators, including Synopsys' (www.synopsys.com) HSPICE, Cadence's (www.cadence.com) Spectre, and Mentor Graphics' (www.mentor.com) Eldo. Users run multiple SPICE simulations and then run the SolidoStat Sampler. The tool employs parallel-processing and proprietary sampling algorithms to provide a threefold to fivefold speedup in Monte Carlo simulation. Running static analysis on SPICE-deck data, the Sampler algorithms create a parametric-yield number and a distribution. If the yield is less than the designer's target, the designer can activate the Characterizer, which uses patent-pending algorithms to pinpoint sources of yield and performance loss in the design, zeroing in on transistor, resistor, and capacitor geometries that designers can change to improve the design. "If there are problems, users can start characterizing their designs to find out what's causing physical distribution, which process variables are problematic, which specifications are problematic, which environmental conditions are problematic, and so on," says Gupta. "It helps designers narrow down the problems in their design so they have to look at only a few variables rather than a few thousand variables."

Once they reduce the field to the problem areas, users can activate the TradeoffAnalyzer, which helps determine whether they can trade off specifications to improve yield. Users can then activate SolidoStat CircuitEnhancer. The tool lists features and suggests sizing alternatives for those features. Designers can then select which features they want to adjust, make those adjustments, and again run Sampler to check yield. The suite runs statically and mines data from the SPICE-simulation database; thus, users need not run a full SPICE simulation and Monte Carlo analysis between each step. The Visualizer tool converts the raw data from all the Solido analysis engines into dynamic visual representations. Prices for the SolidoStat tool suite range from $50,000 to $200,000.

—by Michael Santarini

▷**Solido Design Automation**, www.solidodesign.com.

DILBERT By Scott Adams



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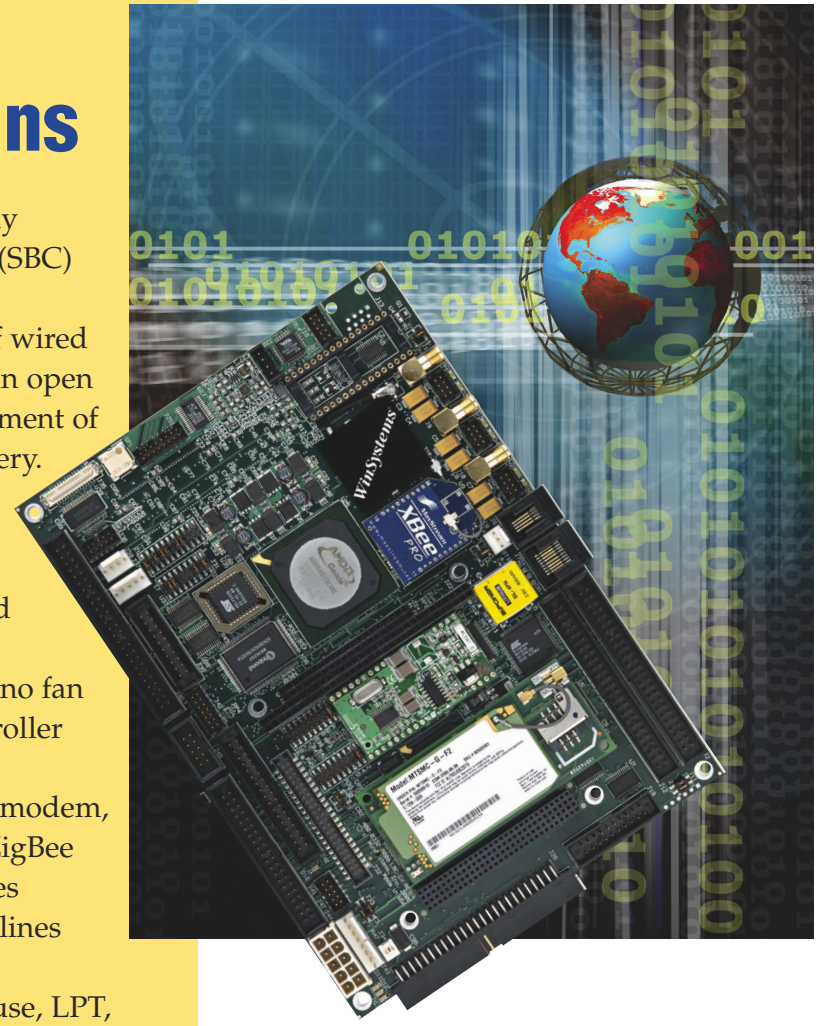

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Serial analyzers enhance comprehensive PCI Express 2.0 testing

Tektronix has announced the TLA7S08 and TLA-7S16 serial analyzers for test and validation of PCIe (PCI Express) 1.0 and 2.0 designs. According to the manufacturer, unlike competing instruments, the new analyzers provide detailed PCIe 2.0 protocol information as well as cross-bus analysis. The units enhance the company's comprehensive PCIe-test approach, which enables the development of next-generation, high-speed computing systems.

PCIe 2.0 introduces performance enhancements for the computer, storage, and communications industries. First among these improvements is a speed increase from 2.5 to 5 Gbps. The most significant validation challenges for PCIe 2.0 are capturing signals at twice the former top speed, verifying power management, and performing cross-bus analysis. Power-management features dynamically negotiate the link width and number of lanes in use—to 16—link speed of 2.5 to 5 Gbps, and idle states to conserve as much energy as possible. Power management is critical—whether in a laptop to extend battery life or in a server system to conserve energy.

The new PCIe protocol uses a three-layered architecture with physical, data-link, and transaction layers and electrical and logical sub-blocks. The physical layer's logical sub-block selects the link width, initializes the bus, and negotiates the data rate. The data-link layer ensures that data sent on the link is correct and that packets are reliably transmitted. The transaction layer constructs requests, completes transactions, and controls transaction-layer packet flow and messaging.

In addition to the serial analyzers, Tektronix is offering new half-width P6708 and full-width P6716 midbus probes and one-, four-, eight-, and 16-lane prerelease slot-interposer probes to test and validate all PCIe 2.0 layers. With narrower links, the P6708's small footprint minimizes board-real-estate requirements. The new analyzers plug into the manufacturer's TLA7000-series logic analyzers, enabling debugging and correlation of general-purpose signals and interconnects, including those to memory and CPUs.

PCIe 2.0 link-width and speed negotiation requires debugging the physical layer's logical sub-block, at which logic-analysis instruments, unlike protocol-analysis tools, provide detailed data. The TLA7S08 analyzer handles unidirectional links as wide as eight lanes or bidirectional links as wide as four lanes; the TLA7S16 analyzer handles unidirectional links as wide as 16 lanes or bidirectional links as wide as eight lanes. You need two TLAS716 analyzers for bidirectional links of nine to 16 lanes. Suggested US prices begin at $55,000 for the analyzers and at $16,000 for the midbus probes.—**by Dan Strassberg**

▷**Tektronix Inc**, www.tek.com.

The TLA7S08 and TLA7S16 modules plug into the manufacturer's TLA7000-series logic analyzers, enabling debugging of the 5-Gbps PCIe 2.0 bus without the need for external deserialization hardware between the probe and the logic analyzer.

DUAL-DISPLAY, 5½-DIGIT DMM'S PRESET BUTTONS EASE REPETITIVE TESTING

Fluke Corp has announced the 8808A DMM (digital multimeter), featuring 5½-digit resolution, multifunction-measurement capability, and a dual display that enables users to simultaneously measure two related parameters, simplifying testing and troubleshooting. The instrument's front panel includes six programmable setup buttons that function much like car-radio presets, allowing production operators to quickly follow a test procedure without pushing multiple buttons. A high/low limit-compare mode with pass/fail indicators can remove much of the guesswork from testing and can help to eliminate production mistakes. Using the setup buttons to invoke pass/fail tests enhances measurement consistency and thus improves the quality and efficiency of manufacturing test. With measurement functions that include volts, ohms, amps, and frequency, the meter also meets performance and flexibility requirements for bench meters in R&D and service applications.

The 8808A exhibits basic dc-voltage maximum error of 0.01% and, according to the manufacturer, is the only meter in its class that features dedicated low-current dc-leakage-measurement capability. The unit uses a high-impedance-input-measurement circuit to make sensitive low-current measurements without loading the circuit under test; in the 2000-μA range, resolution is 100 nA. The 2×4Ω function uses patented split-terminal jacks that allow users to perform four-wire measurements using only two test leads. The optional two-by-four-wire test leads make possible precise, four-wire, low-resistance measurements on miniature surface-mount components. The US list price is $745.

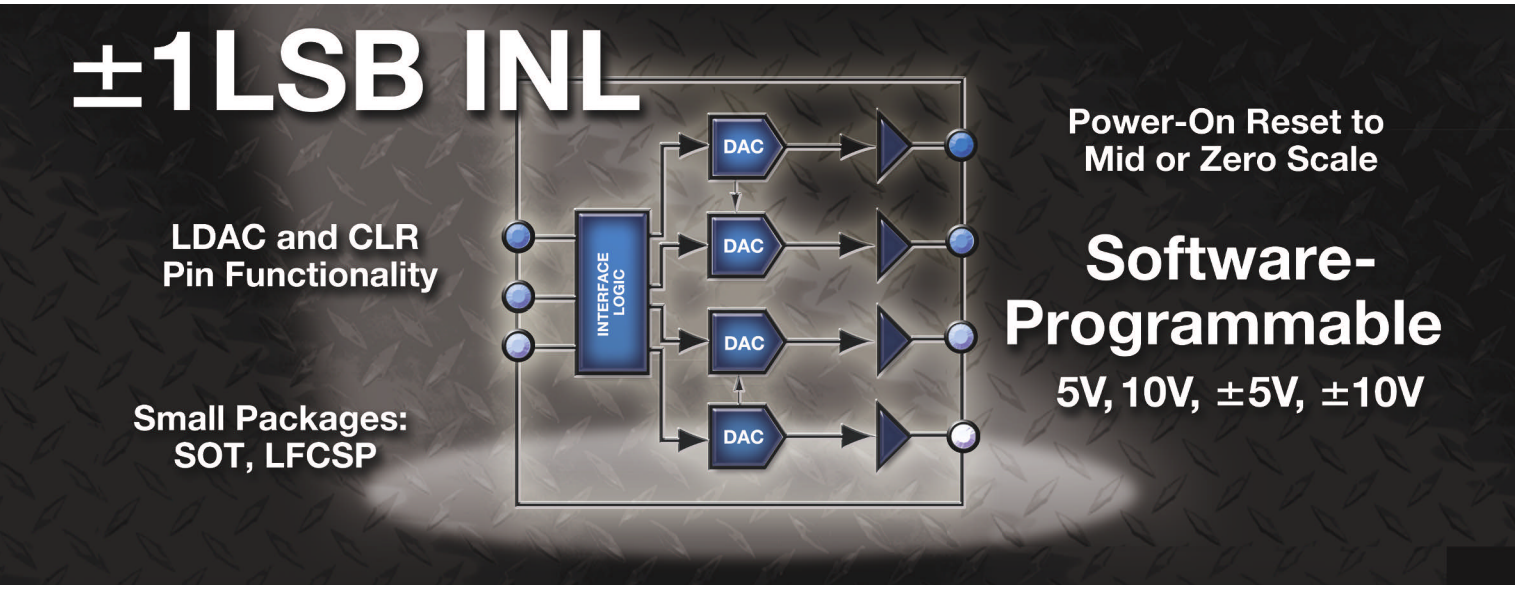
—by Dan Strassberg

▶**Fluke Corp**, www.fluke.com.

The front panel of the 5½-digit dual-display 8808A DMM includes six programmable buttons—just below the display—that you can use, much like car-radio presets, to invoke frequently used measurement setups.

11.08.07

More 16-bit DAC performance for more designs. In process control, analog is everywhere.



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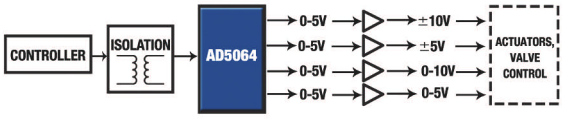
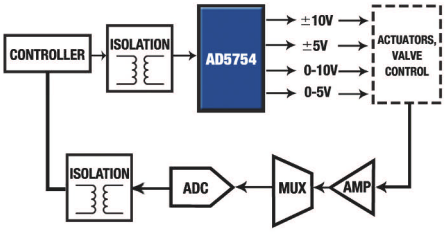


AD5754
Flexible Solution for Closed-Loop Systems

The AD5754 provides a software selectable output range of 5 V, 10 V, ±5 V, and ±10 V for cost-efficient system configuration.



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AD5064	Quad, 5 V, ±1 LSB INL (max), 5 mA @ 5 V	$15.95
AD5764	Quad, ±15 V, ±1 LSB INL (max)	$35.70
Ideally Suited to Closed-Loop		
AD5752	Dual, software-programmable output range of 5 V, 10 V, ±5 V, ±10 V in 24-lead TSSOP	$6.95
AD5754	Quad, software-programmable output range of 5 V, 10 V, ±5 V, ±10 V in 24-lead TSSOP	$10.05
AD5664R	Quad, 5 V, 5 ppm ref, in 3 mm × 3 mm LFCSP	$10.45

All prices shown are $U.S. at 1k quantities unless otherwise noted.
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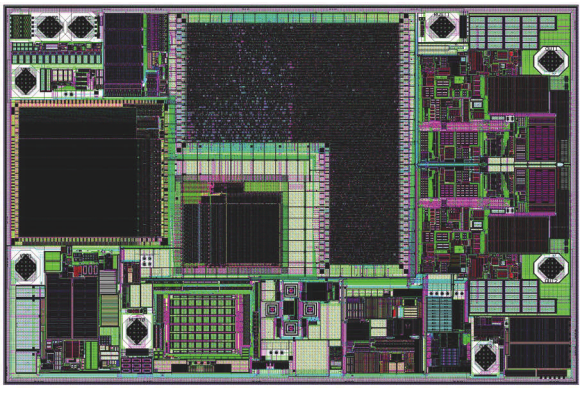
ANALOG DEVICES

Automotive Hall-effect rotary-position sensor uses novel flux-concentrator technology

Melexis uses its expertise in advanced process technology as well as a novel approach to magnetic concentration in the design of the new MLX90316 Hall-effect rotary-position sensor. The eight-pin-SOIC device provides 12-bit resolution and 10-bit accuracy over its temperature range. Because reliability is critical in the device's targeted applications—throttle-pedal positioning, for example—Melexis offers versions of the part that integrate two fully redundant sensors into one TSSOP-16 SMD package.



The Melexis MLX90316 die includes Hall-effect sensors, chopper-stabilized amplifiers, ADCs, a 16-bit RISC processor, DACs, voltage regulators, and output drivers.

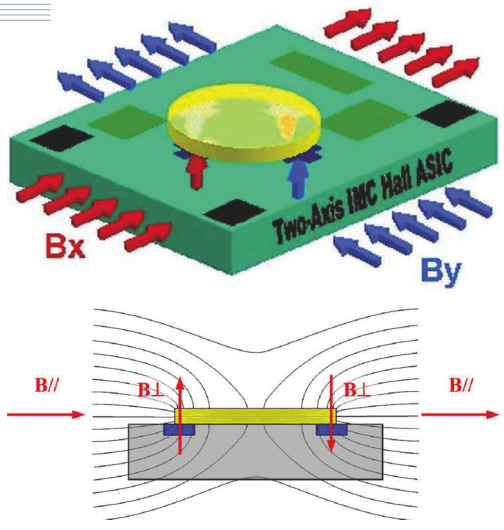
Melexis uses the Triaxis flux concentrator in the magnetic path; the device converts B-fields in the plane of the die into orthogonal fields that penetrate the die. The company applies this concentrator as a back-end deposition to the normal CMOS-process flow. The flux concentrator presents the B-field to the integrated Hall-effect sensor, a differential-analog-signal chain, which includes chopper amplifiers to minimize noise and improve accuracy. The concentrator takes possession of the analog signal. An ADC digitizes the Hall signals, which then go to an on-die-integrated, 16-bit RISC microprocessor. This processor includes filters that users can implement as hysteretic, FIR (finite-impulse-response), and IIR (infinite-impulse-response) devices. The Hall-effect sensor's output has four ranges, allowing manufacturers to do a quick two-point sensor calibration or a more time-consuming three- or five-point calibration for better linearity.

The chip provides PWM and serial-protocol outputs, as well as a DAC to output an analog signal. In addition, a switch output changes level when the sensor reaches a programmable threshold. Self-diagnostics include memory checks, overvoltage and undervoltage detection, and ground-integrity checks. The processor includes a watchdog timer. In addition, the chip self-checks the ADC, the DAC, and the on-board regulator.

The chip suits automotive applications requiring high voltage or the ability to withstand high temperatures in engine-torque, steering-wheel, fuel-level, ride-height, and pedal-position sensors. You can also use the chip in applications requiring rotary or 3-D positions, such as joysticks for entertainment control and seat position. Although the chip's designers had automotive applications in mind, it suits use in industrial and medical applications requiring reliability and temperature range of −40 to +150°C for both the SOIC-8-packaged MLX90316LDC and TSSOP-16-packaged MLX-90316LGO. Prices are approximately $2.40 and $4.56 (10,000), respectively.

—by Paul Rako

▷**Melexis Semiconductors**, www.melexis.com.



The Melexis rotary-position-sensor die has a novel magnetic-flux concentrator that converts magnetic fields parallel to the die into fields that pass through the die.

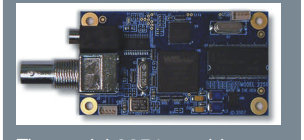
FRAME GRABBER SUPPORTS MOTION DETECTION

For designs dealing with video from an analog source, consider using a frame grabber, which provides a quick and easy way to capture and digitize the video. For example, Sensoray's latest USB model 2251 frame grabber converts an NTSC- or a PAL-composite analog-video source into an MPEG stream along with optional synchronized audio, all in a 1.5×3.5-in. form factor. Users can adjust the resolution and bit rate for picture quality and storage.

You can adjust the output resolution from 320×240 to 720×480 pixels at 30 frames/sec. The bit rate is continuously variable to 6 Mbps. Users can select MPEG1, MPEG2, or MPEG4 compression or can capture frames in JPEG format. The 2251 also supports motion detection in three user-programmable regions of interest. The user can adjust the motion-detection sensitivity and localize the motion to a 16×16-pixel block.

The 2251 includes a software-development kit with support for Linux and Windows. Prices start at $226.—by Warren Webb

▶**Sensoray Inc, www.sensoray.com.**



The model 2251 provides MPEG- and JPEG-video compression to Linux and Windows computers.

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Part Number	Resolution (Bits)	Sample Rate	Max Integral Linearity (LSB/ppm)	SNR, noise rms (dB/ppm of FSR)	Power @ 100 kSPS	Price ($U.S.) @ 1k
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AD7690	18	400 kSPS	±1.5 LSB, ±6 ppm	102 dB, 2.8 ppm	4.4 mW	19.50
AD7691	18	250 kSPS	±1.5 LSB, ±6 ppm	102 dB, 2.8 ppm	4.4 mW	14.50
AD7980	16	1 MSPS	±2 LSB, ±30 ppm	91.5 dB, 9.4 ppm	750 μW	19.50
AD7693	16	500 kSPS	±0.5 LSB, ±8 ppm	96.5 dB, 5.3 ppm	3.6 mW	18.00
AD7685	16	250 kSPS	±2.5 LSB, ±38 ppm	93.5 dB, 7.5 ppm	1.35 mW	6.50
AD7942	14	250 kSPS	±1 LSB, ±61 ppm	85 dB, 20 ppm	1.25 mW	4.75

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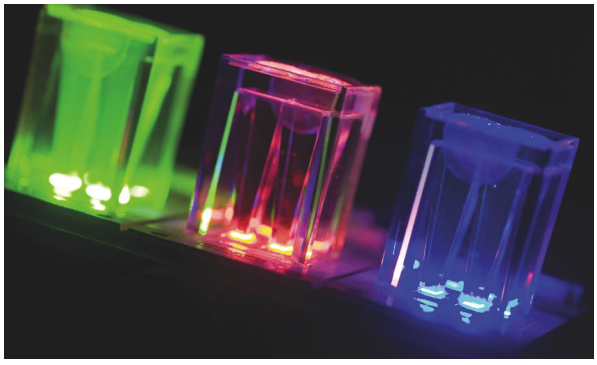
ANALOG DEVICES



Osram's new LED technology combines breakthroughs in device fabrication, optics, and packaging.

RESEARCH UPDATE

BY RON WILSON

Osram, Fraunhofer up for award for their bright ideas

Officials at the German Future Prize (www.deutscher-zukunftspreis.de) have nominated Osram GmbH and the Fraunhofer Institute for Applied Optics and Precision Engineering for this year's award for outstanding technical achievement. The nomination cites the two companies' collaboration in developing new technologies for high-intensity LEDs. The president of the German Federal Republic, Horst Köhler, will present the award.

The development attacks the light loss that traditional LED structures experience. Traditionally, developers manufacture LEDs by growing what will be the light-emitting layer on a substrate, breaking up the devices, and packaging the layer still attached to the substrate. In the new technique, developers grew the light-emitting layer and then coated it with a thin reflective-metal film. The developers then removed the substrate, creating a light-emitting crystalline layer backed by a reflector. They then mounted this film, reflecting layer down, in an optically efficient package, creating an LED that radiates a much higher percentage of its light energy to the outside of the package.

▷**Osram GmbH**, www.osram.com.

▷**Fraunhofer Institute for Applied Optics and Precision Engineering**, www.iof.fraunhofer.de.

AmberWave to research mesoporous materials

AmberWave Systems announced recently that it is entering a joint-research and licensing agreement with the University of California—Santa Barbara for exploration of mesoporous materials. These materials constitute a broad class of engineered materials that include silicas, refractory oxides, carbons, and multicomponent composites, all of which are highly porous. AmberWave builds the materials in single- and double-digit-nanometer pore sizes. Researchers are just now exploring the applications of the materials in electronics, but possible uses include ultracapacitors, advanced batteries, and fuel cells. In general, any electronic device that is sensitive to the exposed surface area of an electrode or the porosity of a membrane could potentially benefit substantially from this previously arcane area of materials science. And the benefits can be huge, at least in capacitor development, in theory multiplying the surface area of electrodes by a large factor for the same-sized sheet of material.

AmberWave, which began life as a gallium-arsenide-technology developer, quickly developed that technology into a strong intellectual-property portfolio in strained silicon. The company also holds a key developmental position in aspect-ratio trapping, a potential way to combine gallium-arsenide and silicon materials to enable, for example, monolithic optoelectronic systems.

▷**AmberWave Systems**, www.amberwave.com.

▷**University of California–Santa Barbara**, www.ucsb.edu.

11.08.07

MOBILE WIMAX MOVES A STEP CLOSER WITH INTEROPERABILITY DEMONSTRATION

Many in the telecom industry view mobile WiMax, the extension of the fixed-WiMax standard to serve mobile devices with broadband connectivity, either as a solid interim step on the way to the full-mobile broadband-4G telephony or as an instance of 4G itself. If mobile WiMax represents a step closer to interoperability, consider that it depends on technologies such as MIMO (multiple-input/multiple-output) transceivers, multiple antennas, and beam-forming algorithms to get as much bandwidth as possible from every connection between the host and the terminal. But these technologies are still emerging, and some question exists about whether base-station and terminal designers are developing compatible technologies.

Fujitsu Microelectronics America and Navini Networks are addressing this question. They recently jointly announced that a Navini Ripwave MX8 base station successfully communicated with a Fujitsu mobile-terminal reference design based on the company's MB86K21 802.16e-2005 chip. The connection employed Navini's Smart WiMax technology and the dedicated-pilot feature that the WiMax standard for Wave-2 mobile devices specifies. It is unclear whether the test was static or allowed motion of the terminal device, but the companies at least completed a connection using the beam-forming technology.

▶**Fujitsu Microelectronics America**, http://us.fujitsu.com/micro/wimax.

▶**Navini Networks**, www.navini.com.

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BY HOWARD JOHNSON, PhD

Aunt Judy: Beware relatives' repairs

Old Aunt Judy approaches you at a wedding reception and, with a halting voice, says, "You know about computers, right? Well, I've got this old eight-track-tape player [or black-and-white television, turntable, or whatever], and it isn't working too well any more. Can you take a look?"

Ridiculous? Yes, but try explaining to her the difference between the high-speed-digital miracles you create at work and the old, transistorized audio anachronism she wants you to fix. You can't. And you don't really want to. Aunt Judy expressed confidence in your abilities, and this is not the time to let her down. Fortunately, I am here to give you some tips. I have a lot of experience in this area. (I have a lot of relatives.)

Rule 1: Unless you have nerves of steel, do the work at home, alone, and away from the supplicant. Take your time.

Rule 2: I know it is difficult, especially with "snap-together"-style plastic cases, but try not to break the case during disassembly. Keep some superglue handy. It must be fresh. I keep mine in the refrigerator. For most plastics, I like the kind of cyanoacrylate glue—typically sold under trademarks such as Superglue and Krazy Glue—that comes with a glue activator.

Rule 3: Don't lose any parts. Sweep the floor *before* you start work. I work on a table top made of white-board material. I write a note by each little pile of screws that says where they go, and I tape the screws to the table top. Plastic bags and baby-food jars work just as well.

Rule 4: Take pictures with a digital camera. You will later thank yourself if putting the product back together becomes confusing.

Rule 5: Test one small section of the product at a time. This step usually requires a signal source to stimulate each section and a detector to observe its output. When working on audio products, for example, I use a small voice recorder as the signal source and a sensitive pair of headphones, with a preamplifier if necessary, as a detector. If you have an ac-coupled headphone, you can use it to "listen" to hum on the dc-power rails.

Rule 6: Cheat. If the product was once popular, you can probably find the schematics for it online. This rule has a subrule: Never promise a fix date. You need time to find those schematics, advice, or whatever.

Rule 7: Buy a replacement on eBay. *Do not give Aunt Judy the replacement*, because she will know that it isn't hers. The new one will have scratches in different places. Just use the replacement as a benchmark, comparing the broken set against the original in every particular. The replacement also gives you a source of spare parts. When you are done, throw it away. You are not building an economically efficient repair business here, just saving some face—and, possibly, impressing your cute cousin.

Rule 8: In older transistorized products, the problem likely involves conductive dirt, corroded connectors, or a power-supply malfunction—that is, unless someone has dropped or spilled milk into the product. So, blow out the dust with a can of compressed air, scrub the board with a cleaner from CRC Electronics (www.crc-electronics.com), polish all the connections, and check the power supplies. Those steps will fix 90% of your problems. For the other 10%, you can go on the Web to buy replacement drive belts and needles for any turntable. And plenty of people still sell old CRTs, and, yes, you can still buy eight-track tapes.

Rule 9: To solve a power-supply problem, first substitute a good external supply. If the PCB (printed-circuit board) does not indicate the correct dc-supply voltage, then set your external voltage at approximately 60 to 80% of the rating printed on the bypass capacitors in the circuit. By the way, old capacitors become highly unreliable as they age. Some people just replace them all as a precautionary step.

Rule 10: Never accept Aunt Judy's money. Doing so will lock you into a lifetime of repair work with your whole family. Instead, trade her for something she's really good at—like baking cherry pies. EDN

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Go to www.edn.com/071108hj and click on Feedback Loop to post a comment on this column.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

It's how Logitech reinvented the remote control.

Harmony 1000

Imagine if you could turn on the TV, start the movie and set up the sound all with one touch of your finger. Imagine one touch to all your entertainment. That's what Logitech imagined. To create their newest activity-based universal remote control, Logitech turned to Freescale. Freescale i.MX applications processors enable multi-functionality with low power consumption, and helped Logitech create a scalable board for future generations. By working with Freescale, Logitech literally put all our entertainment at our fingertips, and made the world a smarter place. freescale.com/smarter

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BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Building bridges

Technological innovation during the second half of the 20th century came at an unprecedented pace, and, unlike earlier times, many advances during this interval moved rapidly into the broad consumer market. Because our society, until that time, tended to wring the full value and lifetime from a consumer good, marketers needed to generate sufficient excitement for new products to cause customers to switch in advance of necessity: the origin of the disposable economy.

Starting in the 1950s, advertising copy used phrases such as "jet age," "atomic age," and "Space Age" to connect products to a societal image of emerging and rapidly changing modernity. Ironically, perhaps, none of these phrases had much staying power save one: the "digital age," which, beginning in the 1970s, correctly suggested that associated goods weren't simply modern but were manifestly different from products of earlier times.

Indeed, the digital abstraction has revolutionized our industry, almost every sector of our economy, and all but a few aspects of our lives. Though the effects have been quite real, this abstraction is, as all are, strictly conceptual. As a result, virtually every product design must bridge the digital abstraction and the real analog world.

Virtually every product design must bridge the digital abstraction and the real analog world.

This requirement is remarkably fractal-like: Layout considerations within an IC, the interface between an IC and its PCB, the PCB's layout, the product interface to points beyond the box, systems of boxes, and networks of systems all must contend with essentially similar interface concerns. This observation holds despite these items' enormously different scales, which can span more than 10 orders of magnitude. It is also the case that, though interface challenges grow with bandwidth, the issue arises throughout the spectrum.

A few considerations early in the design phase can focus an interface design. A consequence of the fractal-like traits of interfaces is that you can begin specifying interface requirements at the product-definition phase and refine them at the block-diagram, schematic, and simulation phases.

I distinguish this process of design refinement from iterative design—design refinement being a purposeful process of design in phases, and iterative design being a sequence of design repairs. The first pass at the product-definition phase should allow you to establish a good rough estimate for an interface's cost, complexity, and design time. The first phase's output can serve as your check as an implementation takes shape at the block-diagram phase. Disparities in cost or complexity estimates from the first and second phases serve as warnings against one of three conditions:

- The interface design is heading off into the toolies.
- The first phase failed to account properly for all product-definition requirements.
- Changes to the product definition have made obsolete the cost and complexity estimates, and these estimates require updating as part of your project-management activities.

Make similar checks at subsequent design phases.

As a phase-one starting point, bear in mind the signal-source, -line, and -client attributes for each interface. Despite your signal's "digital" significance, remember that interface behaviors are analog and multiparametric. Take into account each line's bandwidth requirement, source impedance, signal magnitude, and run length; the characteristics of the connecting media; and the presence of noise sources or interferers, all in the context of the receiver-side circuit's signal-fidelity requirements. In the simulation phase, compare the transmitter- and receiver-side waveforms under the worst-case combination of these measures. Consider pre- and post-signal-conditioning techniques to correct deficiencies. If you delay these observations until prototype evaluation, you may slip from design refinement into a more costly course of iterative design. EDN

Contributing Technical Editor Joshua Israelsohn writes about analog and power applications and technologies. Contact him at jisraelsohn@ieee.org.

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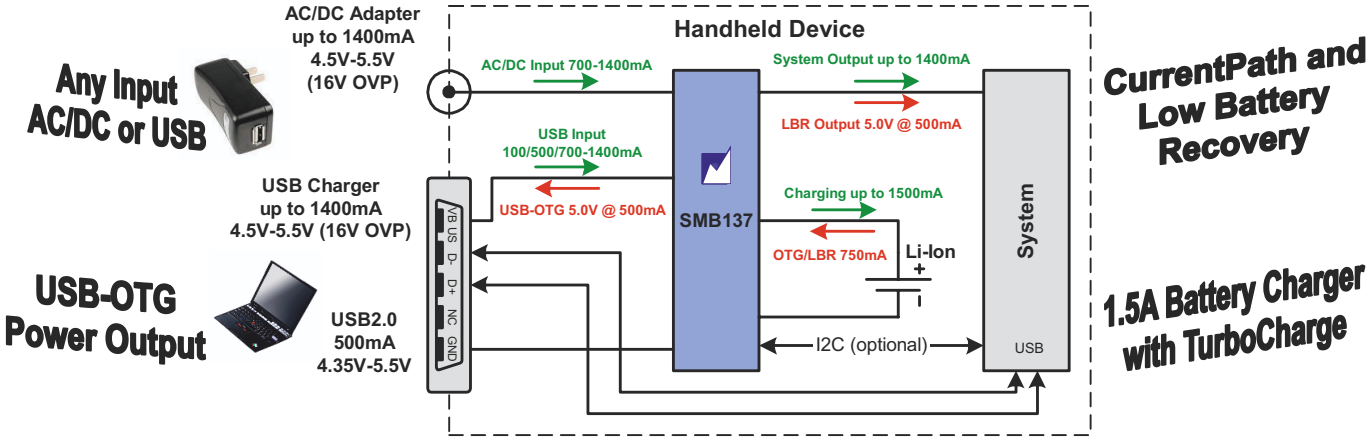

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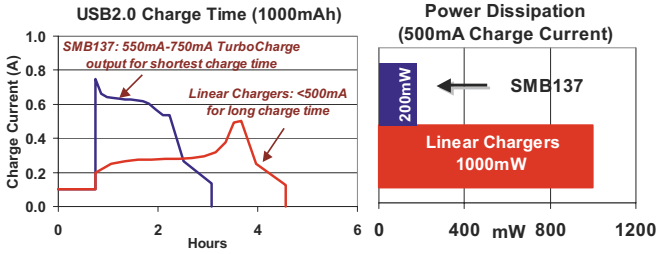

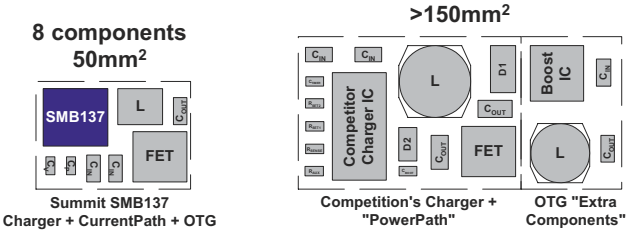

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BY JOHN LINSTROM • S&K ELECTRONICS AND SUNSPOT

What color is 10 kΩ?

DANIEL VASCONCELLOS

In the '80s, I worked for a company that made industrial computers in an STDBus format. (It soon went to a single-board-computer format.) My first major project was to migrate the ADC on its ADC/DAC multi-I/O card from 12 to 14 bits. The card design was flexible: It could handle 16 single-ended or eight differential inputs, each over a range of 0 to 5V, 0 to 10V, ±5V, or ±10V, with an onboard cold junction for thermocouples. The ADC inputs and eight-output, 12-bit DAC were individually strap-programmable. Conversions and updates were in the 100-kHz range, all under the control of an 8051 with a 64-kbyte EEPROM and 32-kbyte SRAM. So far, so good.

I found a multisourced ADC and did some front-end work—the input amps were LM324s, and the error budget was wide. There were many choices for lower-offset and lower-temperature-drift parts at nearly the same price. The layout of the programming straps was not intuitive, and the user manual got a few tweaks. We went through an artwork spin and prototype build just fine, but when we fired up the board, it gave us 11 bits of solid data, maybe 12 on a good day. I finally narrowed down the problem to microprocessor churning during analog-to-digital-conversion cycles. We switched to a CMOS 8051, put the digital side to sleep, and let the "end-of-conversion" flag wake up the microprocessor. Now, the team had 13 to 14 bits of solid data over the whole input range and could honestly brag about greater resolution in the trade magazines. Orders followed, salesmen were happy, and life was good.

It was good, that was, until we couldn't properly test and calibrate the first batch of 25 boards. Now, the eager customers and smiling salesmen started turning up the heat. The team scoped, metered, substituted parts, studied the artwork, and checked the golden board—following the drill every design engineer knows by heart—all for naught. My handmade board worked great, but all the production copies tested in the weeds.

We used 4051-style data latches for the channel selects, and I had normalized-gain-set resistors with values of approximately 10 kΩ. The value was high enough to swamp any changes in switch resistance, low enough to keep down resistor noise, and high enough to keep bias currents and self-heating low. Plus, it made the math easy. (In those days, we still used through-hole parts.)

Staring at the good and bad boards finally gave me the "smack upside the head." The 10-kΩ-resistor code, as every good design engineer knows, is brown-black-orange followed—you hope—by a tolerance band. The bad boards were stuffed with a mix of 10-kΩ and 300Ω resistors! I had stared at the problem so long, expecting something immense, that I had blown right by the obvious. Backtracking the trail of destruction unraveled the whole tale. The people who built the units didn't know resistor codes from Morse code; they stuffed in whatever was in the correct pick bins. The stockroom used kits from bins that incoming inspection filled. My computer bought from reputable distributors but reserved incoming tests for items more costly than 2-cent resistors. I checked the stocking bins and found a 60/40% mix of 10-kΩ and 300Ω resistors. We were thankful that no other bins fell prey to the same confusion. We had a heart-to-heart talk with the buyers, engineering staff, and production team. I don't think anyone learned the resistor color code that didn't already know it, but everyone learned how to identify correct parts. EDN

John Linstrom is a design engineer with S&K Electronics and works for his own company, Sunspot, in his spare time. Like John, you can share your tale and receive $200. Contact Maury Wright at mgwright@edn.com.

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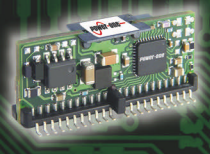

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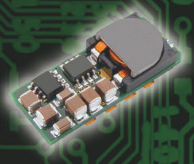

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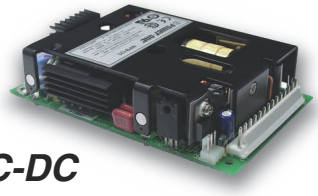

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GREENHORNS IN THE HIGH-END-FPGA MARKET, LATTICE AND ACTEL ARE SHOOTING IT OUT AGAINST OLD HANDS XILINX AND ALTERA IN THE BATTLE FOR LOW-COST DEVICES.

High noon for FPGAs:

LOW-COST-VERSUS-HIGH-END SHOWDOWN

BY MICHAEL SANTARINI • SENIOR EDITOR

Although the market for high-end, high-priced SRAM-based FPGAs has matured into a gentlemanly duel between FPGA veterans Xilinx Inc and Altera Corp, the emerging low-cost-FPGA market has turned into the FPGA industry's version of the *Gunfight at the OK Corral*. Companies including Lattice Semiconductor and Actel Corp are fighting it out with each other as well as with Xilinx and Altera, increasingly adding advanced functions—traditionally the province of high-end, high-priced FPGAs—to their low-cost-FPGA families. In the very-high-end-FPGA market, customers mainly have a choice between either Xilinx's Virtex devices or Altera's Stratix family. In the low-cost-FPGA market, however, customers have many more choices and benefit from the stepped-up competition between the many vendors fighting it out for FPGA revenue. Today, customers can buy 1 million-gate FPGAs with high-speed I/O and processor or DSP capabilities for much less than $100 in low volumes and for tens of dollars in high volumes.

This competition has benefited users but has—and at least temporarily—come at the expense of the FPGA industry's overall revenue. The media has widely covered the FPGA industry's success at the ASIC market's expense, replacing sockets that ASICs traditionally held. During the past year, however, the FPGA industry has had a dose of its own medicine, as the low-cost-FPGA market has quietly begun to take socket wins—and, thus, revenue—away from the high-end-FPGA market.

Bryan Lewis, research vice president with research company Gartner, notes that the FPGA industry has since 2002 sold a steadily increasing number of devices. However, Gartner predicts that

the FPGA industry will show a decline this year, due in part to low-cost FPGAs' replacement of sockets that high-end FPGAs traditionally held. "Low-cost-FPGA units are ramping fast, but their lower ASPs [average selling prices] are clearly having an impact on the dollar growth of the overall FPGA market," says Lewis. "In fact, we now forecast 2007 FPGA/PLD [programmable-logic-device] revenues to decline 1.9%." That anticipated decline is not due entirely to FPGA-industry cannibalism, he says. In 2007, the FPGA market underwent "the perfect storm," says Lewis, simultaneously experiencing inventory, customer-consolidation, and pricing issues. He expects overall FPGA/PLD-market revenue to come roaring back in 2008 to post 14.4% revenue growth (**Figure 1**).

But the two biggest upstarts—and, some would say, spoilers—in the low-cost-FPGA market are Actel and Lattice, which are maintaining their push to add high-end functions in their low-cost devices, putting severe price pressure on Xilinx's and Altera's high-end FPGAs. Both Actel and Lattice claim that the large FPGA vendors have traditionally deliberately withheld high-end functions from their low-cost FPGAs to force users to buy their typically three-times-more-expensive high-end FPGAs. Both upstarts claim that the high-end-FPGA vendors are starting to buckle under the pressure, and one of the first signs of this surrender is Altera's latest product introduction, the 90-nm Arria GX. The upstarts claim that Arria GX is simply a 90-nm Stratix II GX device with a different package. Although Altera concedes that it based Arria GX on a Stratix II GX architecture, the company says that the Arria GX lacks some of the features and performance of the Stratix II GX device. The company claims that it merely slimmed down the Stratix II GX to meet the right mix of performance, power requirements, and price to fulfill the needs of the market with the Arria GX. The Arria GX's price falls between the company's low-cost Cyclone and its high-end Stratix devices. "Lattice has changed the playing field for the SRAM guys," says Martin Mason, director of silicon-product marketing at Actel. "It's a market that Actel has not historically played in. But Altera and Xilinx have sold a lot of high-end devices into the market for high-speed I/O, and Lattice went in there overnight and took out one digit from the amount people could charge for high-speed SERDES [serializer/deserializer] products. I'm sure Xilinx and Altera are furious over the impact that [move] is having on the high-end business."

Mason believes that the high-end-FPGA vendors are now experiencing a classic example of the innovator's dilemma (**Reference 1**). "You have this market, you're getting fat and happy in it, and someone comes in with a disruptive technology and starts taking market share away from you. Do you go in and try to compete with them by lowering your prices? If you do, then you actually trash the market that has gotten you where you are," says Mason. "All of us in the FPGA market have been doing that to the ASIC market, but both we and Lattice have little to lose and everything to gain by introducing disruptive technologies against the Big Two in FPGAs."

Xilinx and Lattice are not throwing in the towel, however. Neither is content to simply replace high-end-FPGA sockets with low-cost FPGAs, and neither plans to reduce the prices of their high-end FPGAs to fend off competition from low-cost FPGAs. Each instead hopes to serve markets that FPGAs have not traditionally served (see **sidebar** "Low-cost FPGAs seek new markets").

AT A GLANCE

- Low-cost FPGAs generally target use in products, rather than as FPGA-prototyping vehicles.
- Xilinx introduced the first low-cost FPGAs in 1998 and reports that Spartan has produced $2.1 billion in cumulative revenue with a compound-annual-growth rate of 36.2% from fiscal year 2000 through 2006.
- Customers are now replacing high-end-FPGA sockets with low-cost-FPGA sockets in much the same way that FPGAs once displaced low-end ASICs.
- Research company Gartner predicts that FPGA/PLD (programmable-logic-device) revenues will decline 1.9% in 2007, due in part to FPGA cannibalism.
- Low-cost FPGAs are fine for some applications, but some FPGAs require extra power circuitry that may add to the overall cost of a system.
- Customers should also take into account the FPGA vendor's EDA-tool set when shopping for low-cost FPGAs.

A LITTLE HISTORY

In 1998, Xilinx introduced the first low-cost FPGAs, the Spartan family, and aimed it squarely at replacing ASICs for production parts. Before the product's

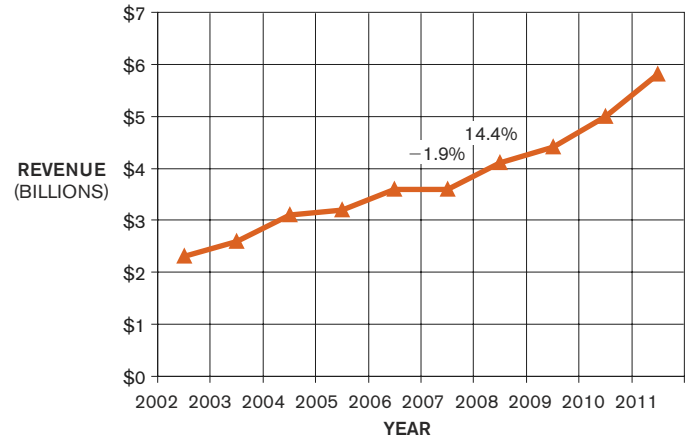

Figure 1 Research company Gartner predicts that FPGA/PLD revenue will decline 1.9% in 2007 in part because low-power FPGAs are taking market share away from high-end FPGAs. But Gartner predicts that the FPGA revenue will spring back to grow 14.4% in 2008.

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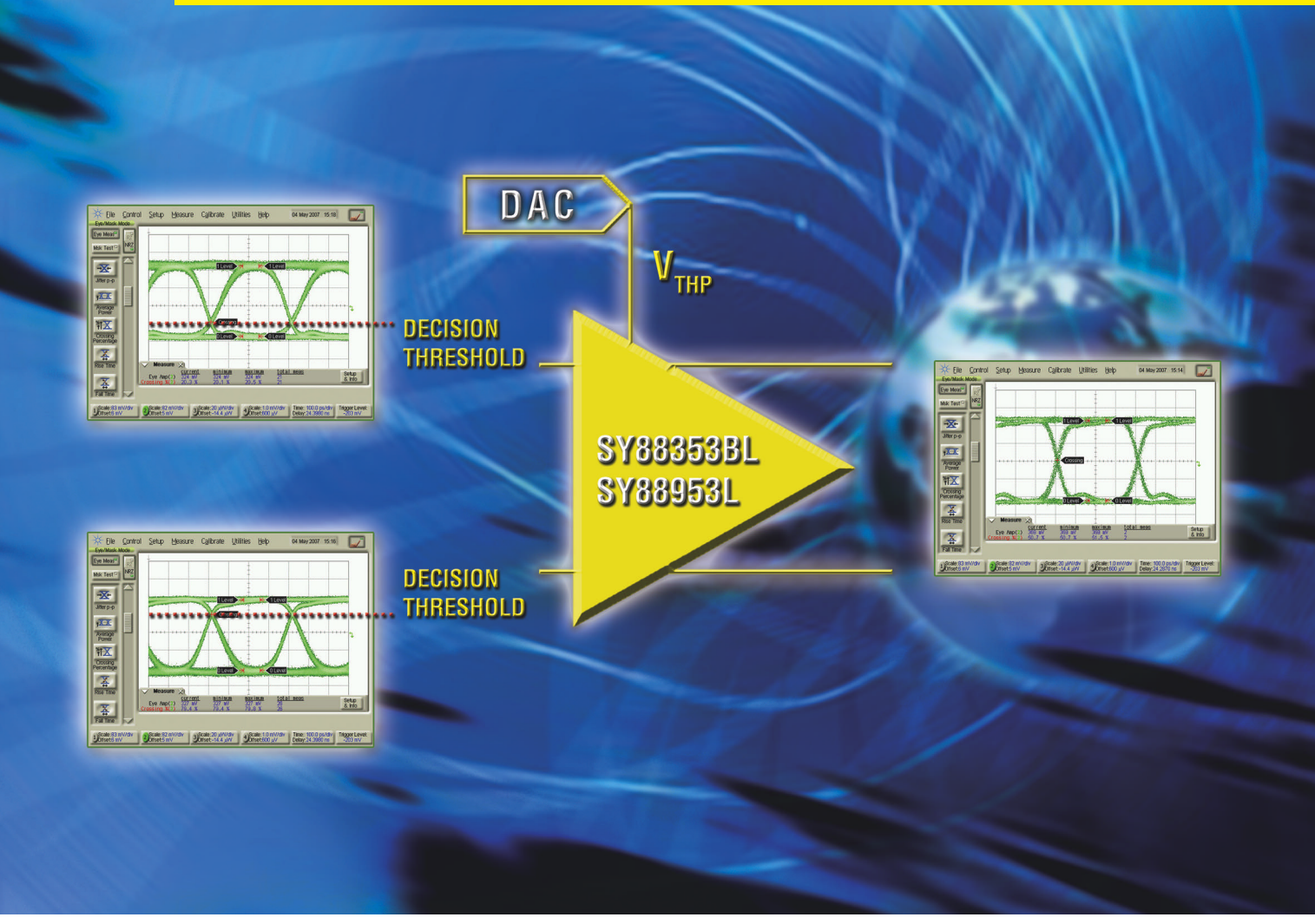

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release, IC-design engineers had used FPGAs mainly for prototyping ASIC designs and would ultimately implement those designs in cheaper, faster, higher capacity ASICs. In those days, PLDs lacked the performance, capacity, and power requirements for use in end products, and, more important, they were too expensive. At the time, many PLD vendors also offered low-cost CPLDs (complex PLDs), but performance and capacity limitations hampered—and still hamper—those parts. Still, some customers used them in sockets that older and less sophisticated ASIC devices traditionally held.

The Spartan family, however, opened a new market and offered formidable capacity, performance, and numbers of functions at a reasonably low price and thus started to displace midrange ASICs in end products. This scenario was especially true in applications that required versatility and reprogrammability and those requiring too few units to justify the cost of spinning an ASIC. Xilinx has shipped more than 230 million devices worldwide, according to Mark Moran, senior strategic-marketing manager for the General Products Division at the company. Those sales have yielded $2.1 billion in cumulative revenue with a compound-annual-growth rate of 36.2% from fiscal year 2000 through fiscal year 2006.

THE SPARTAN FAMILY OPENED A NEW MARKET AND OFFERED FORMIDABLE CAPACITY, PERFORMANCE, AND NUMBERS OF FUNCTIONS AT A REASONABLY LOW PRICE.

As foundries have introduced semiconductor processes that are more difficult to manufacture and more expensive to design, both the low-cost-FPGA and the high-end-FPGA markets have grown and have grabbed more sockets away from the ASIC market. When Xilinx jumped into the low-cost-FPGA market, Altera, Actel, and Lattice soon followed. The first devices they offered were traditional sea-of-gate devices that consisted mostly of reprogrammable logic. But, as new market opportunities opened, most of the FPGA vendors started to add hard-wired functions, such as microprocessors; DSPs; memory; high-speed SERDES; and support for popular interfaces, such as PCIe (Peripheral Component Interconnect Express), to their architectures to capture specific markets and one-up competitors in not only the ASIC market, but also the FPGA market.

The low-cost-FPGA shoot-out has indeed escalated the size, performance, low-power requirements, and number of advanced functions these devices have, yet they maintain a price that allows

LOW-COST FPGAs SEEK NEW MARKETS

SRAM FPGAs found their first big successes mainly as glue logic, helping ASIC designers add functions at the last minute that they accidentally omitted, for example, or facilitating communication between processors and memory in telecom and networking systems. FPGAs vendors then started adding RapidIO blocks to their FPGA architectures and realized further success in markets such as telecom and communications. They then added processors, DSP capabilities, and security.

You can now find low-cost FPGAs everywhere–at home, in your automobile, at work, and in various industries, according to Mark Moran, senior strategic-marketing manager for the General Products Division at Xilinx. The market for consumer products, such as set-top boxes, is now perhaps the biggest market for FPGAs. It was also one of the first segments in which Altera saw big success with its low-cost FPGAs, according to Danny Biran, senior vice president of product and corporate marketing at the company. "Customers in this market traditionally release 10 or more models a year, and they can customize FPGAs to suit not only each product line, but also each unit," he says. For example, each TV manufacturer can use FPGAs to fix pixel, color, or shading problems on a case-by-case basis. The devices also find use in data conversion for modems and set-top boxes. "The next generation of devices in these areas will become even more integrated and require even more FPGAs," say Moran, noting that some TV vendors are starting to include DVR (digital-video-recording) functions in their HDTVs (high-definition televisions).

FPGAs have also found great wins in the automotive market. Initially, FPGAs counted success in GPS (global-positioning-system) navigation and back-seat DVDs in a mix of after-market and OEM products. However, as vendors offer more nonvolatile devices to their lineups, low-cost-FPGA use in automobiles is expanding beyond infotainment and GPS units. For example, Actel's products are now finding use in automotive backup-safety systems, cameras, and power-train systems. In most of these cases, FPGAs are displacing ASICs or eliminating the need for multiple discrete devices on a PCB (printed-circuit board), saving board space. In others, low-cost FPGAs are replacing high-end FPGAs.

The market for systems that operate in the ISM (industrial/scientific/medical) frequency band is probably the biggest battleground between high-end FPGAs and low-cost FPGAs. The big trend in this area is toward wireless and battery-powered systems, so the requirement for low power consumption plays a large role. "It forces customers into a value-based play because the high-end-FPGA power hogs use a lot of static and dynamic power and are unsuitable for applications that are going portable for the first time," says Mason.

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customers to justify using the devices rather than ASICs, standard-cell ASSPs (application-specific-standard products), or implementations that combine discrete functions on PCBs (printed-circuit boards). Creating low-cost FPGAs for emerging markets is difficult, and all the players offering low-cost FPGAs say it's a balancing act to keep raising the bar on performance and features in ever-more-expensive process technologies. They must achieve this goal while keeping prices low enough that customers will find their devices attractive as production parts, rather than as prototyping parts for ASICs.

It's a balancing act for FPGA customers, too. Although an FPGA may have a lower per-unit cost than an ASIC, customers must look closely at each device's system requirements. Actel's Mason, for example, is quick to point out that SRAM FPGAs remain power hogs and typically require users to add extra power-control circuitry and power bricks to their PCBs to run SRAM FPGAs.

MOST FPGA-MARKET PUNDITS WILL LIKELY AGREE THAT THE FPGA INDUSTRY AS A WHOLE IS TODAY FIELDING A BRILLIANT ARRAY OF LOW-COST DEVICES FOR A GROWING NUMBER OF APPLICATIONS AND MARKETS.

Some also need external boot-up memory, which may require users to buy an external boot device or to increase the boot-up requirements of their targeted processors. Customers for SRAM-based FPGAs must also heed the rule of 80%; that is, they must buy an FPGA that has 20% more gates than they require if they intend to hit the FPGA vendor's advertised performance grade (**Reference 2**). Altera's senior vice president of product and corporate marketing, Danny Biran, and Xilinx's Moran, also point out that EDA software is a big differentiator in this market and that the smaller vendors' design software lags behind the offerings of the big vendors. Biran also notes that transceiver-targeted FPGAs typically add complexity to users' system designs; thus, FPGA vendors attacking this market must also offer software to help designers adequately program the devices into their systems. "If you look at the vendors offering these types of devices and then you look at the software they offer with the devices, it's again a Coke-and-Pepsi market," says Biran, referring to the long-standing so-called Cola Wars between Coca-Cola and Pepsi (**Reference 3**), an analogy describing the situation when two companies—in this case, Xilinx and Altera—dominate a mature market.

Although designers should be aware of some facts when shopping for devices in the low-end market, most FPGA-market pundits will likely agree that the FPGA industry as a whole is today fielding a brilliant array of low-cost devices for a growing number of applications and markets. **Table 1**, available at the online version of this article at www.edn.com/071108df1, lists the latest low-cost-FPGA offerings from Actel, Altera, Lattice, and Xilinx. "You can get a lot of cool stuff for less than $20," says Actel's Mason.

THE OLD-TIMERS

First, take a look at what the old hands have to offer. Xilinx offers the Spartan, Spartan-2, and Spartan-3 generations of its high-pin-count, high-density, low-cost-FPGA device. With the introduction of each successive generation, Xilinx has broadened its portfolio to capture new markets. Of the FPGA vendors offering low-cost FPGAs, Xilinx has the broadest portfolio, fielding five versions of its 65-nm SRAM-based Spartan-3 family and multiple densities and speed grades for each version. The logic-optimized Spartan-3E is a traditional sea-of-logic-gates FPGA. The Spartan-3A targets I/O for high-speed applications, and the Spartan-3A DSP targets DSP applications. The newest addition to the lineup is the Spartan-

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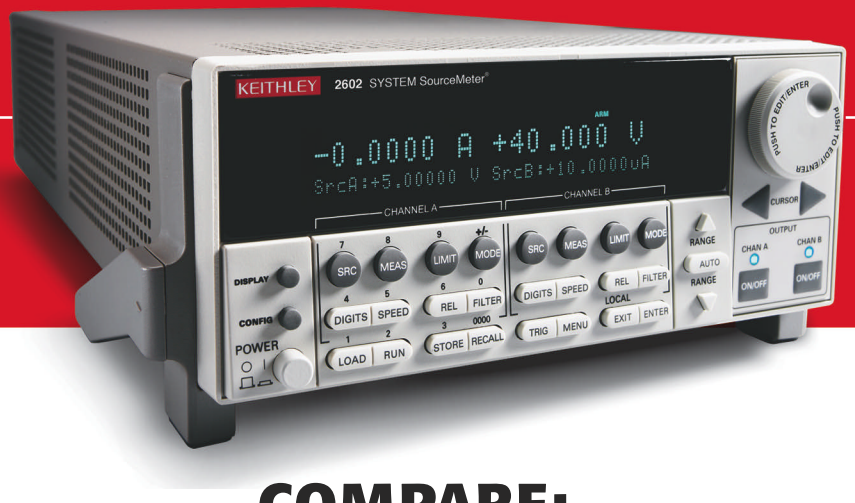

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3AN, which is essentially a Spartan-3E that Xilinx couples with a flash on an SIP (system in package) for nonvolatile-system applications. Although each device targets its own market segment, each shares flexible power-management modes for low cost, along with "device-DNA" security technology, which helps customers prevent theft of their designs.

As for the other veteran in the market, Altera offers its low-cost, SRAM-based Cyclone FPGA family, which debuted in 2002 in a 130-nm-process technology. The company in 2004 introduced the 90-nm Cyclone II and, in 2007, the Cyclone III in TSMC's (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) 65-nm LP (low-power) process technology. As of press time, Altera offered eight speed grades of its Cyclone III products ranging from 5000 to 120,000 logic elements, with as much as 4 Mbits of embedded memory and as many as 288 DSP multipliers running at 260 MHz.

This year, the company also introduced its Arria line of FPGAs to target users needing reprogrammable devices with highly functioning, relatively low-cost transceivers. Arria GX has a higher price and better performance than Cyclone because it supports three protocols: PCIe, GbE (Gigabit Ethernet), and SRIO (Serial RapidIO).

Arria GX and the high-end Stratix II GX use the same logic fabric, transceiver technology, and process technology, but they differ in a number of ways: Arria GX is slower and is available in lower cost packages, and its transceivers support speeds of only 2.5 Gbps and have fewer functions. For example, Arria GX devices lack support for adaptive equalization, a feature you'll find in Altera's high-end Stratix II GX.

ENTER THE UPSTARTS

Lattice jumped into the low-cost-FPGA market at the end of 2002 with its 130-nm ECP (Economy Plus) family. The company last year followed up that introduction with the 90-nm ECP2 family and then this year with its ECP2M family. ECP2M adds two significant high-end features to the low-cost-FPGA market: hard-wired 3-Gbps SERDES and as much as 5 Mbits of on-chip memory, supporting DDR and DDR2 I/O, SPI (serial-peripheral-interface) 4.2 I/O, and hard-wired DSP support. Lattice also offers the XP and XP2 families, which debuted in 2005 and February of this year, respectively. The XP2 family marries an SRAM ECP2 architecture with a bank of flash memory on one die. "We are trying to make the SRAM-based FPGA plus its associated boot-flash memory about the same price as its equivalent nonvolatile product," says Gordon Hands, director of strategic marketing an Lattice, who notes that the XP is similar to Lattice's original ECP family and that the XP2 is similar to the ECP2 devices but with slightly smaller density.

While Xilinx, Altera, and Lattice battle it out in low-cost, SRAM-based FPGAs, Actel, which offers flash-based devices, is content to broaden its low-cost-FPGA-market reach into applications requiring security and low power

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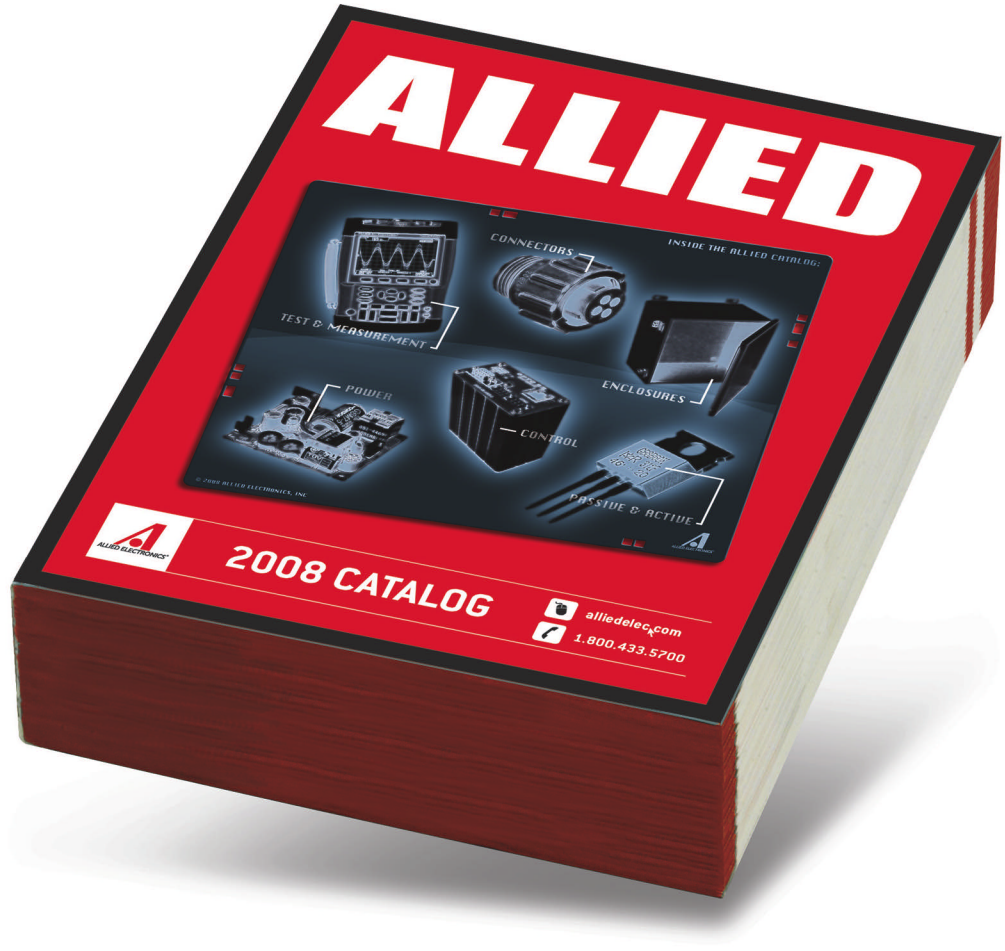

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For more on FPGAs, see David Marsh's article, "Low-cost kits: the new FPGA-designer trend," at www.edn.com/article/CA6391429.

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consumption. Flash-based FPGAs have traditionally been slower than SRAM-based FPGAs, but flash-based devices consume less power and are more secure than SRAM-based devices. The company's low-cost ProASIC3 FPGA focuses on the combination of low power, security, and relatively high density and is available in seven versions, with densities of 30,000 to 1 million system gates. The company based its flash-based Igloo FPGA family, which debuted last year, on the ProASIC3 but with added modes to further reduce power. The smallest device in the Igloo family, the AGLO30, can operate on as little as 5 μW, and the largest device operates at less than 1 mW, which is two or three orders of magnitudes lower than its SRAM competitors.

Actel also has an agreement with ARM (www.arm.com) that allows users to place a hardened ARM7 core on Actel's FPGAs for very-low-power use. "When you put an ARM processor on the device, you can get as low as 24-μA standby current for that implementation. The business model allows Actel to provide the ARM processor to customers free of royalty, licensing, and price," says Actel's Mason.

Quicklogic no longer considers itself an FPGA vendor, but its low-power PolarPro and ArcticLink CSSPs (customer-specific standard products) are worth mentioning. The one-time-programmable devices function as extremely low-power "sandman" devices—turning off power to parts of handheld systems when they are not in use, thus conserving a given system's overall power consumption. The PolarPro devices boast 10 μA of static-power consumption, 15 mA of active-power consumption, and 10 μA of dynamic-power consumption. ArcticLink devices essentially marry a PolarPro programmable array with hard-wired functions on a die targeting markets for low-power systems.

THE MEASURE OF SUCCESS

Overall, in recent years, the FPGA industry has done remarkably well taking share away from the ASIC market and giving users a very-low-cost and relatively stable alternative for quickly designing innovative next-generation products. Historically, customers, the media, and the financial community have measured FPGA-vendor success by a company's ability to be first to market with high-end devices on the latest silicon processes. However, as companies such as Lattice and Actel introduce low-cost devices with high-end features and increase pressure on Xilinx and Altera to follow suit, industry participants may soon define FPGA success by a vendor's ability to serve emerging markets with the right mix of features, performance, power savings, and price that customers find reasonable for production use. EDN

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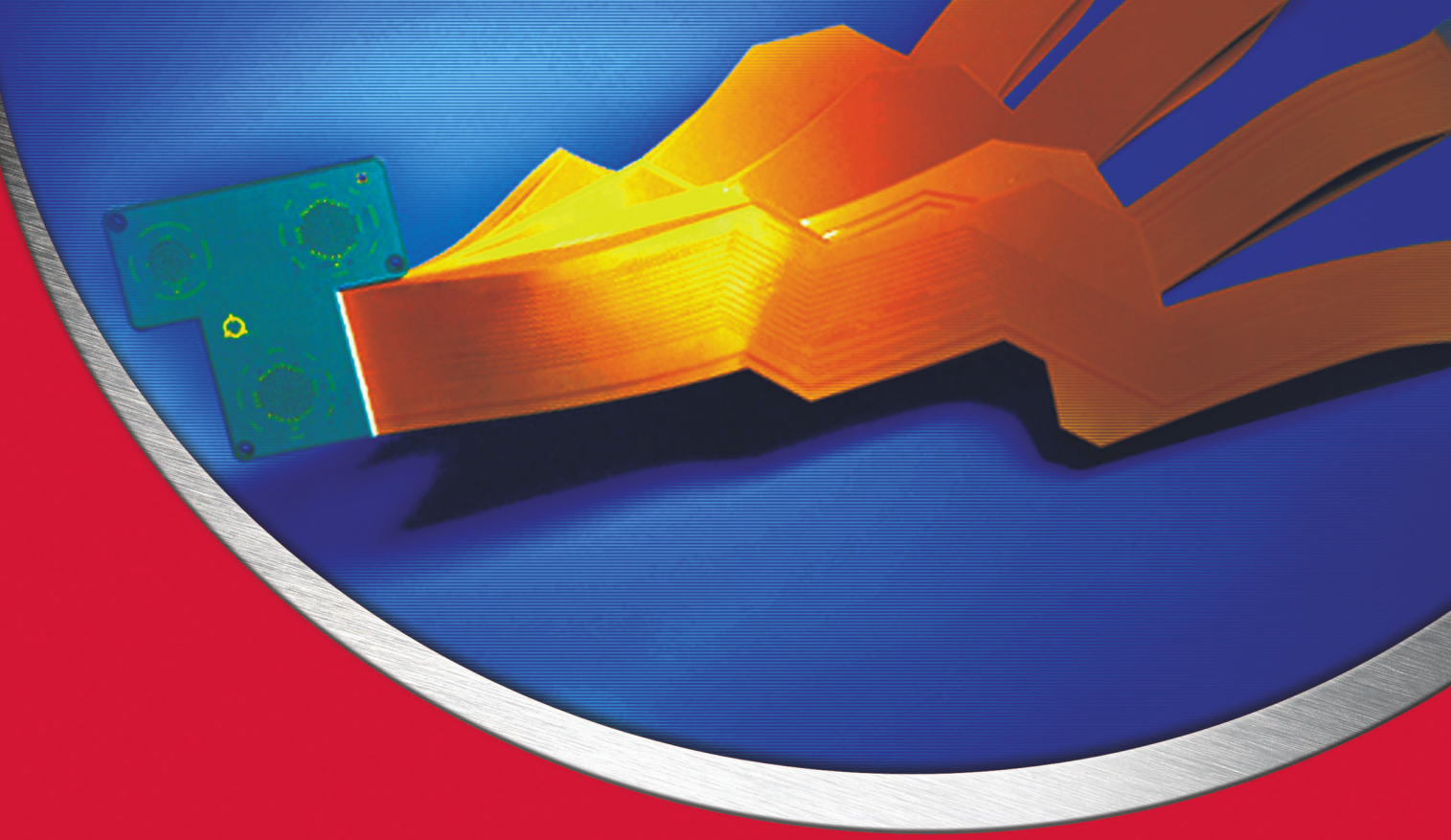

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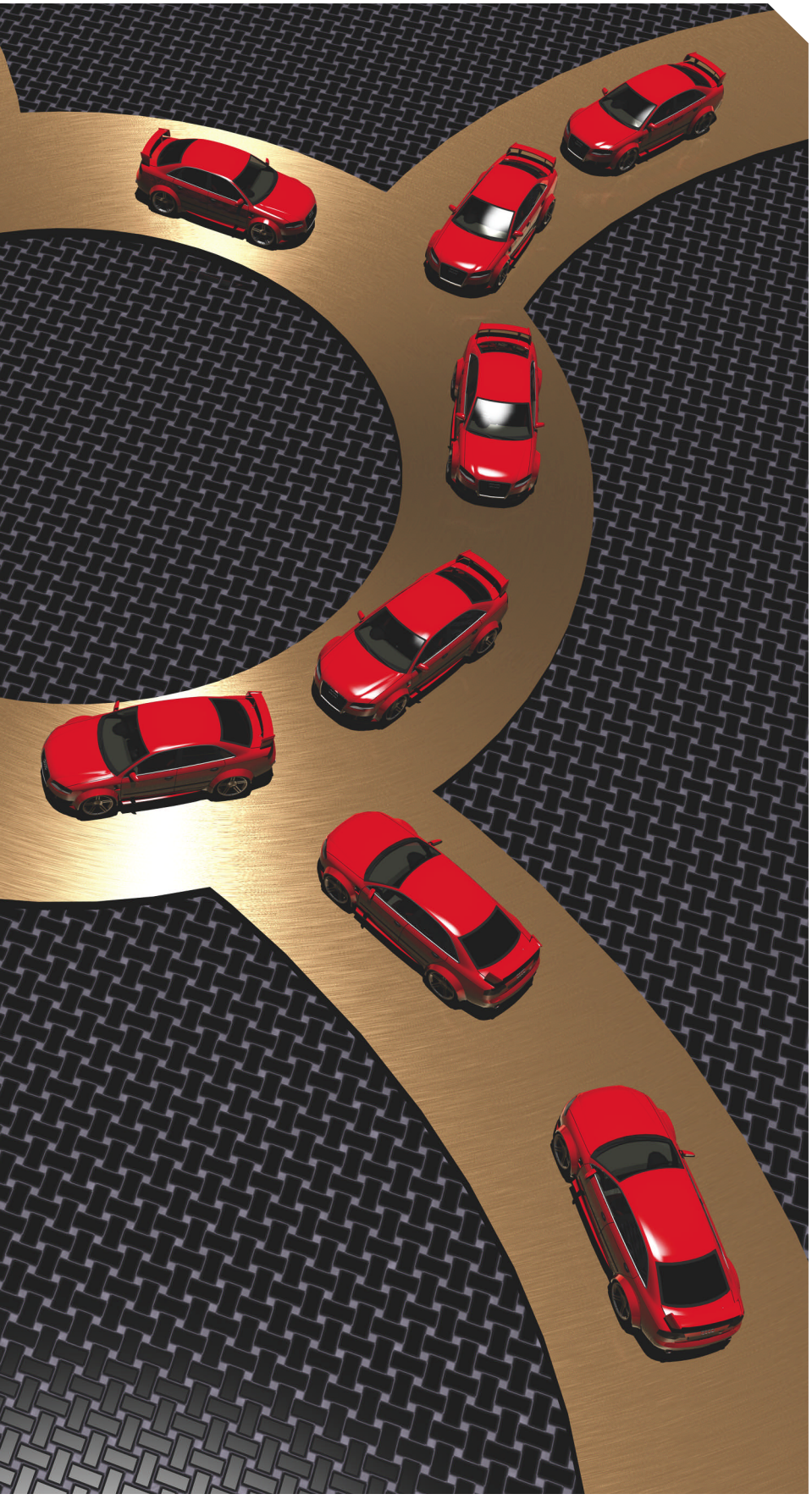
BY RON WILSON • EXECUTIVE EDITOR

The SOC (system on chip) began life in the image of the board-level computers that preceded it: as a central processor that a CPU bus connected to local memory and peripheral controllers. That CPU-centric, bus-oriented architecture has since been the underlying plan for many SOCs. But integration has brought complexity in the form of complex peripherals with their own DMA (direct-memory-access) controllers, coprocessors, and additional central processors, all on the same die. Accordingly, the interconnect architecture of SOCs is changing. The old CPU-centric bus is fast retreating to within the functional blocks of the chip; multiple buses, specialized point-to-point links, and on-chip networks are replacing it.

TRAFFIC MANAGEMENT: A GROWING NIGHTMARE FOR SOC DESIGNERS

CONNECTING THE BLOCKS ON SOCs IS BECOMING A PRIMARY PROBLEM IN ADVANCED-CHIP DESIGN.



Change is rapid, and architects are nearly unanimous in worrying that the change has far outrun the tools necessary to support it. "Today, we still see a number of classic SOC designs, with an ARM core, peripherals, and a memory interface," observes Hugh Durdan, vice president of marketing at ASIC supplier eSilicon. "Even when these designs grow to include multiple processing cores, they often stick with the classic AMBA AHB [Advanced Microcontroller Bus Architecture Advanced High Performance Bus] structure."

But there are growing indications that the centralized-bus approach to SOC interconnect is simply running out of steam (see **sidebar** "Is the problem bus bandwidth or processor bandwidth?"). This problem appears to be partly architectural. As the number of processing nodes on a chip increases and as the data traffic that those nodes generate or consume grows and becomes more varied, the simple demand for raw bandwidth becomes a problem (**Figure 1**). Yes, it is possible with nine layers of metal and statistical-timing tools to give a multimaster bus almost-arbitrary bandwidth. But the costs in layout complexity, signal-integrity analysis, power consumption, and congestion—especially in this day of stringent design-for-manufacturing rules—make this approach nearly intractable.

In part, too, the problem involves tools. The classic tool for provisioning the classic SOC bus is, to put it bluntly, Microsoft Excel. In simpler times, architects could just add up aggregate-bandwidth requirements of the blocks on the bus, add in a bit of head room to account for times of peak congestion, and use the sum to determine the necessary bus bandwidth. Available bus bandwidth so exceeded the needs of individual blocks that a problem was almost mathematically impossible.

But those days are gone. "You really can't tell anything from aggregate-bandwidth estimates any more," warns Silistix's vice president of marketing, David Lautzenheiser. Just as the centralized bus

is rapidly giving way to more complex interconnect architectures, the spreadsheet is yielding to a more complex brew of system-level modeling, statistical tools, and cycle-accurate models that the skill and patience of the architects bind together.

ASSESSING THE PROBLEM

Aggregate bandwidth isn't the right question, and a centralized bus isn't always the right answer for two main reasons. First, traffic can differ enormously in its characteristics. Second, functional blocks can differ just as much in their data and timing needs. The problem of analyzing and provisioning on-chip interconnect is not a matter of providing enough for everyone to be happy but rather providing just the right kind of interconnect between just the right blocks. Often, you can achieve that goal with a bus. If you can't, myriad other techniques present themselves. A multimedia SOC well illustrates the variety of data flows a designer must face. To begin with, a CPU will usually turn up somewhere. That CPU will produce at least two data flows with distinctive signatures: the continual fetching of new instructions and the sporadic two-way traffic of load and store operations.

Caches in the CPU block usually modify this traffic pattern. So, the traffic pattern from the CPU core is a random scattering of bursts as the caches empty or fill lines. This scenario differs greatly from the traffic signatures that emerge from other devices. A baseband signal in a radio SOC, for example, looks like a word or two of data at regular—sometimes very short—intervals from an ADC. Video entering from a camera or DVD player looks similar. But the intermediate data that the video-compression engine pushes to local memory can look like a series of macroblocks that the engine stores and loads in a nearly random sequence rather than a stream of pixels that the scan line organizes. Each type of data has a natural signature. And, as in the case of CPU cores, local memory and state machines can alter this signature.

BANDWIDTH AND LATENCY

Just as kinds of traffic have signatures, kinds of functional blocks have personalities. CPUs, hard-wired signal-processing pipelines, video encoders, serial ports, and DRAM interfaces all have different needs and wants. Despite all the focus on the bus bandwidth surrounding them, "processors are notoriously sensitive to latency, though their bandwidth requirements are modest when compared with some of the bandwidth hogs," observes Gideon Intrater, vice president of solutions architecture at MIPS Technologies. A CPU's cache controller may not often ask for data, but, when it does, the whole CPU may be sitting there waiting.

In contrast, some functional blocks are just interested in raw bandwidth. "These [products] include high-performance networking devices—PON [passive optical networking] is a great example—video engines, such as MPEG encoders in DVD recorders and H.264 decoders in HDTVs, and imaging engines, such as the rasterizers in printers and the JPEG encoders in digital cameras," Intrater says. "Fortunately, in most systems, the bandwidth hogs are less sensitive to latency, and processors that are sensitive to latency are not much in the way of bandwidth hogs."

Beyond this distinction, there are blocks with special requirements. Imaging or video processors that work with discrete cosine transforms typically process pixels in macroblocks—often an 8×8-pixel square of information—and so need to be able to easily load and store these blocks without explicitly gathering or scattering the pixels across a scan-line-oriented memory.

But the grand prize for fussiness has to go to that ubiquitous memory element, the DRAM. With a complex synchronous interface and a segmented memory array that imposes a signifi-

AT A GLANCE

- SOCs (systems on chips) are outgrowing centralized-bus-based architectures.
- Accurate use models are vital to understanding traffic patterns.
- A combination of ESL (electronic-system-level) and cycle-accurate approaches is necessary to understand interconnect.
- As SOCs evolve, interconnect modeling will become mandatory.

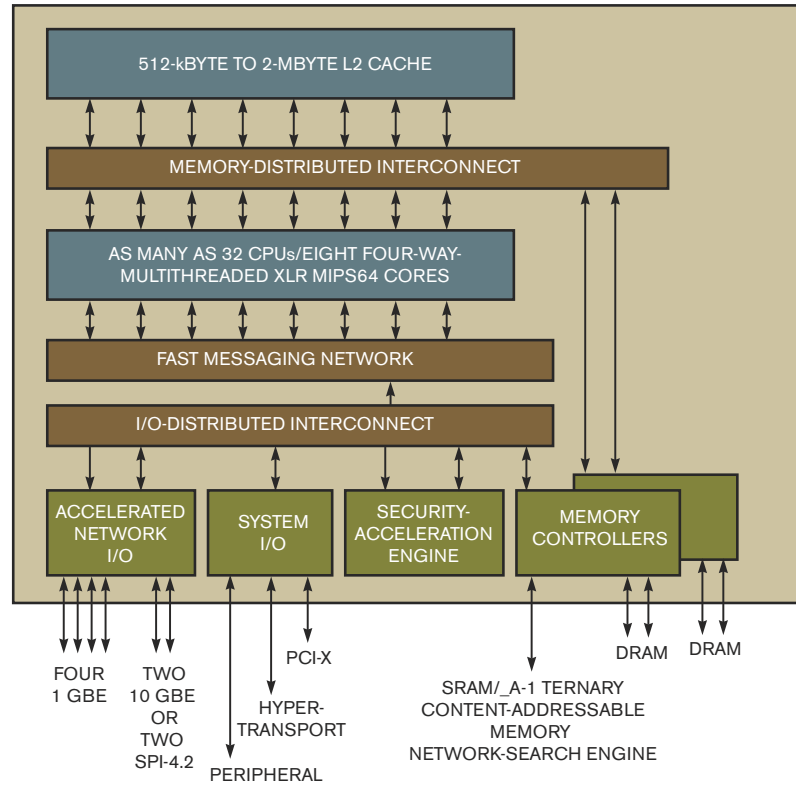


Figure 1 Raza Microelectronics' XLR processor architecture suggests how far SOCs have departed from the classic CPU-centric, bus-based interconnect scheme.

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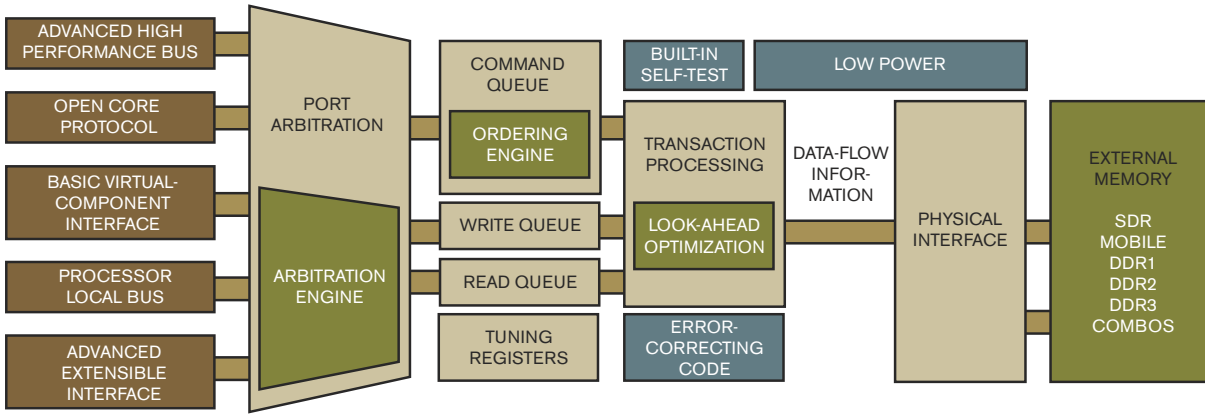

Figure 2 Today's high-end DRAM controllers have become list processors with queuing, reordering, and quality-of-service functions.

cant latency for issuing requests in the wrong sequence, DRAM offers an effective bandwidth that can vary enormously, depending on how you access it. In many cases, only one organization of read and write requests can provide anything close to theoretical throughput. Unfortunately, although these strict requirements are reasonably well-matched to the traffic pattern from a CPU's L2 cache controller, they don't even resemble the aggregate-traffic pattern when several dissimilar processors are all sharing a DRAM port.

In simple language, then, the goal of interconnecting architecture is: Adapt the traffic patterns to the needs of the client blocks so that all data arrives in adequate time with minimum expended energy. Within the constraints of the architects' knowledge of the traffic and

IS THE PROBLEM BUS BANDWIDTH OR PROCESSOR BANDWIDTH?

By Chris Rowen, Tensilica Inc

As communications and media-stream data rates increase, most chip designers quickly recognize that data bandwidth is a key factor in design success. Tensilica's experience with more than 100 multiprocessor-chip designs suggests some basic ideas to untangle the bandwidth confusion.

For example, inadequate data communications causes a shortage of raw bandwidth–the total sustained-bandwidth demands for data communications for I/O, off-chip memory, and bandwidth between on-chip blocks exceed the maximum sustained bandwidth of the interfaces. It also causes excessive latency. The worst-case or typical latency for access to data causes data starvation under some important circumstances, such as when inadequate overall bandwidth adds contention latency.

The bottlenecks in communications appear in multiple places in the design. The three most common locations are at the off-chip memory controller; across the on-chip bus, especially when there are multiple masters, particularly processors and DMA controllers, accessing multiple slaves (memories and I/O interfaces); and at the interface between the processor and the bus.

The processor-bus bottleneck relates to the peak data-transfer rate across the interface, which is often close to the peak on-chip bus bandwidth. The bottleneck also relates to the rate at which you can move data from remote memories across the on-chip bus or from off-chip; into local memory; into and out of processor registers; through local memories; and out to remote memories. With a traditional RISC processor accessing data across an on-chip bus, this data movement might take 10 to 20 processor cycles per 32-bit data word, even if the data is already on-chip and the processor does not modify the data along the way.

You can break the processor-bus bottleneck in two ways. First, using a second bus master, such as another processor or a DMA (direct-memory-access) controller, to move the data into and out of the first processor's local memory can partially relieve the bottleneck. However, RISC's 32-bit registers and load-store register remain problems. Second, you can extend the processor interface to permit high-bandwidth data streams to bypass the bus-interface bottleneck. Processors with direct-connection ports and queues can move an order-of-magnitude more data through processor execution units than RISC processors.

Bus and nonbus interconnect can work in harmony in complex chip designs. Best practices suggest that, when a designer knows that a pair of subsystems requires high interconnect bandwidth and well-bounded latency, he should establish an optimized path between them. Other communications, including communications of the two sensitive subsystems, can safely use a common multimaster/multislave on-chip bus for less bandwidth and latency-sensitive data movement. This separation retains the generality of the common bus but reduces the risk of contention surprises, eases modeling, and enhances performance scalability of the platform.

Optimizing communications for the high-bandwidth links also helps energy efficiency. Direct connections, such as processor-to-processor-communications queues, often use 10 times less energy per data transfer than the equivalent bus-based transfer.

AUTHOR'S BIOGRAPHY

Chris Rowen is president and chief executive officer of Tensilica Inc.

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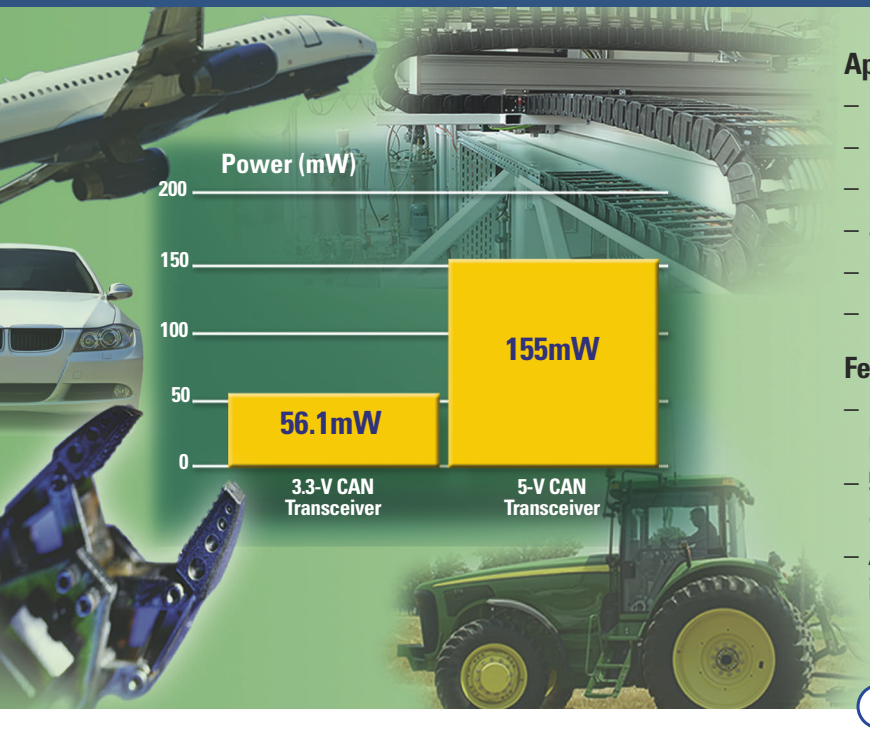

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TEXAS INSTRUMENTS

clients and the power of their tools, this description fairly depicts what happens today. But those are serious constraints. The first problem is that, to understand traffic patterns, the architect must understand usage models for the completed system, Lautzenheiser points out. "Use profiles are important here, and they involve the intangibles of user perception. In a handset displaying video, the criterion for success may not be how many megabytes per second a bus delivers to the video decoder, but rather whether the user thinks his display seems to twinkle. Predicting such qualitative user perceptions requires searching out those unanticipated use models that put the most stress on the system interconnect. And [completing this task] before you can put a physical prototype in the hands of a real user requires system-level modeling."

In fact, this area may be the one place in system design in which the elusive ESL (electronic-system-level) tools have established a firm role. "It is best if the system architects can begin modeling data flows even before the IP [intellectual-property] blocks themselves are fully defined," says Charlie Janac, president and chief executive officer of interconnect-IP company Arteris. "The data flow in a real sense defines the chip."

With these ideas in mind, Lautzenheiser and other experts suggest an architectural design flow that begins at the conceptual level: What blocks should connect to what? From this simple connection diagram, the flow then attempts—using ESL modeling of the blocks and the best possible information on use models—to quantify the data flows as to volume, signature, and client requirements. Finally, the architects attempt to prove that the on-chip interconnect meets these criteria. But this process is iterative. "There are always surprises," Lautzenheiser says. "The trick is to have an easy path between architectural design and implementation so that you can iterate quickly, and an underlying scheme that is extensible enough to accommodate changes without major architectural revisions."

LINKING AND SHAPING

There are two fundamental tools for building the on-chip network: links and shaping resources. Links provide a data pathway between blocks. You can implement them as a portion of a shared bus, as a dedicated connection, as a pathway in a switched network, or in more creative ways. Shaping resources include caches, FIFOs, queuing engines, and reorder buffers. Perhaps the easiest way to move from a classic CPU-bus architecture to a more powerful approach is to segment the buses. "In media SOCs, you can [achieve this goal] by dividing the traffic into low-latency transactions, high-bandwidth transactions, and less critical peripheral transactions," suggests Janac. Then you can provision each type of transaction separately, even if doing so means multiple bus connections on some blocks. Brian Gardner, vice president of IP products at Denali Software, points out that this approach not only places each type of traffic on a physical medium appropriate to it, but also connects data flows that you can model in similar ways, substantially increasing modeling accuracy for the resulting link.

The result of this process is often a hierarchy of interconnect links, Lautzenheiser says. This result is rather clearly visible in the Raza Microelectronics network processor (**Figure 1**). A similar pattern emerges when you look inside some functional blocks—for instance, at the interconnect within a modern CPU, such as the ARM Cortex A9. Here, private links connect the processing core to its L1 instruction and data caches. A multimaster, high-speed-cache bus, in turn, connects the L1 caches to an L2 cache serving as many as four processor cores. Additional links for control and snooping logic lurk in the background. Two system-bus connections come from the L2 controller.

But what happens when it's impractical to provide an appropriate physical link for each data flow? An excellent example is the SOC's DRAM controller, which must take in whatever mix of traffic the multiple processors on the chip throw at it but must somehow mold that cacophony into the highly ordered stream of commands acceptable to a DDR DRAM. To get a look at the complexity of the problem, look inside one such controller (**Figure 2**). This sample

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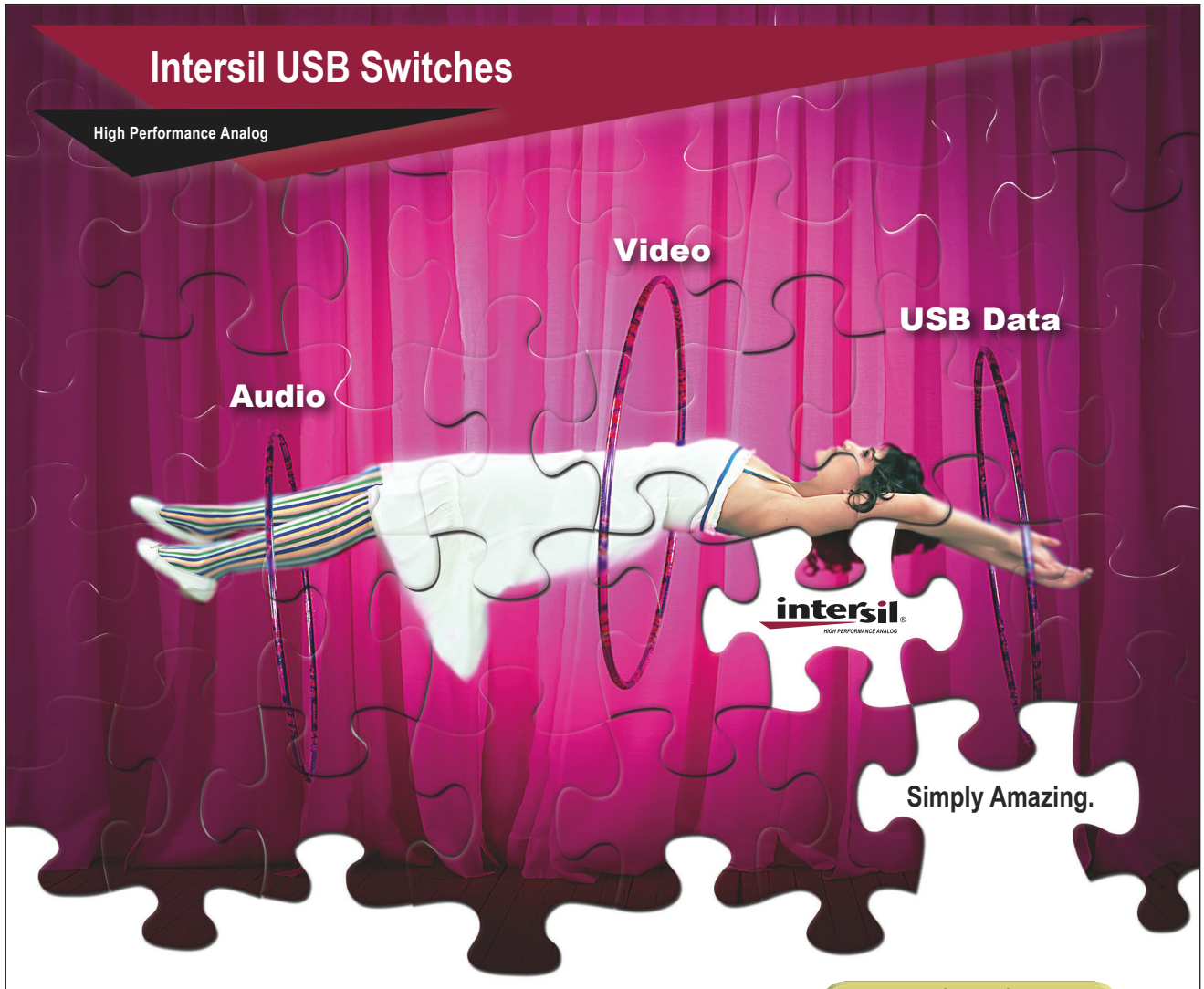

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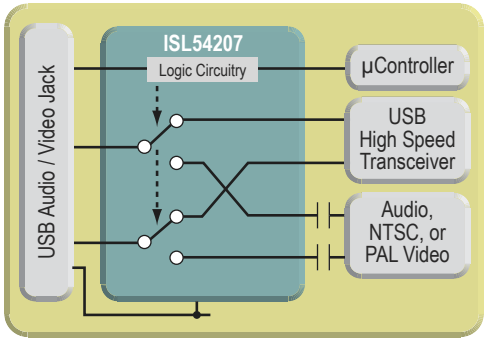

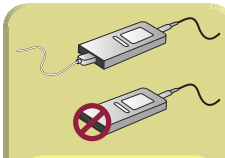

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ISL54417	0.007	12	0.04 / 0.03

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Device	Audio THD 32Ω (%)	USB Speed
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device processes transactions in a number of discrete stages. First, an arbitration engine determines access to the controller based on a priority scheme. Then, the controller loads requests into command, read, and write queues, in which they await reordering based on quality-of-service needs and the realities of DRAM timing. Finally, the requests pass through a transaction-processing engine that looks ahead into the queues to reorganize and gather requests for optimum DRAM usage.

Versions of the same thinking are becoming more and more common in other functional blocks. Often, signal-processing or encoder/decoder blocks contain sophisticated DMA engines that provide many of the same functions as a DRAM controller—scatter/gather processing, reordering of data, and buffering to turn random requests into bursts. The engines perform these functions not so much to please the DRAM controller—in fact, they may puzzle the DRAM controller—as to adapt the traffic to the physical link over which it must travel.

RESULTS AND FUTURES

The result of all this work can be substantial. The result of SOC tuning can improve system performance by a factor of four or five times for basically the same functional blocks, according to MIPS President and Chief Executive Officer John Bourgoin. When you put it into perspective, this magnitude of acceleration is more than you can get from a CPU upgrade or a faster process and even more than sometimes results from adding a hardware accelerator.

As SOC architectures move from functionally divided heterogeneous multiprocessing toward semisymmetric multiprocessing, the need for focus on interconnect architecture shifts from a performance-enhancement and energy-saving alternative to a mandatory part of system design. Without a detailed analysis of data flows, a dynamic multiprocessing system may simply require more interconnect provisioning than an affordable silicon design can offer.

And that possibility brings us back to the tools question. Today, Lautzenheiser says, the tool flow for architects—if they are not still working with white boards and spreadsheets—is an ad-hoc combination of ESL-modeling tools, statistical analyses based on queuing theory—which can give a good overall picture but may completely miss corner cases—and cycle-accurate models that can explore corners but may be too slow to find them.

"You need architecture-level modeling," Arteris' Janac agrees. "The problems have become too complex for a spreadsheet. But at ESL, there's no reality to even the best tools—they represent an abstraction. So, you have to bind your system-level explorations to cycle-accurate models of your IP."

One way to do this binding, MIPS' Intrater suggests, is the use of hardware emulation. "The cycle-accurate models are based on RTL, and they are far too slow for booting Linux or running an application. The state of the art today is to manually combine coarse-grained statistical tools with cycle-accurate simulations. But if you have RTL models of the interconnect at an early enough stage, you can use emulation to run billions of cycles through cycle-accurate models."

This state of the tools preserves architecture as art. Modeling a scheme at the right levels, having accurate use models from realistic users, looking in the right places for critical cases, and making accurate conclusions from the cycle-accurate models are still—despite the gradual emergence of system-level tools, especially from interconnect-IP providers—matters of art and experience. But it is an art that has grown increasingly vital, and, as we move into the age of large multiprocessing systems on dice, it will be indispensable. EDN

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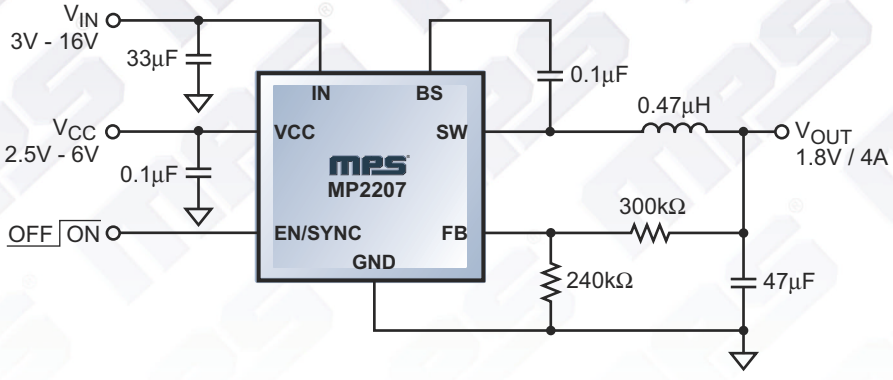

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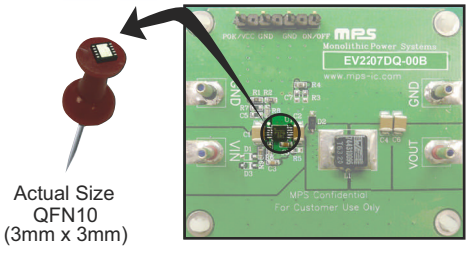

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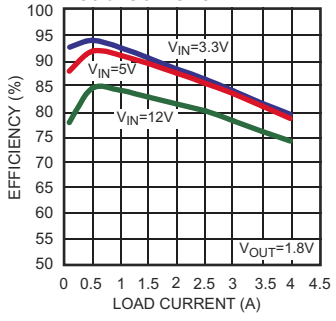
MP2207	1.3MHz	91% @ 1.5A	80mΩ	3.0 - 16	0.8 - 0.9 x VIN	4	QFN10 (3x3)
MP2119	1.5MHz	93% @ 1A	100mΩ	2.7 - 6.0	0.8 - 0.9 x VIN	2	QFN10 (3x3)
MP28128	1.5MHz	95% @ 1.5A	60mΩ	2.7 - 6.0	0.8 - 0.9 x VIN	2.5	QFN10 (3x3)

Other High Voltage Non-Synchronous Bucks

Part	Frequency	VIN (V)	VOUT (V)	IOUT (A)	Package
MP4459	4MHz (Adj.)	4.5 - 40 (Max)	0.8 - 36	1.5	TQFN10 (3x3)
MP4460	4MHz (Adj.)	4.5 - 40 (Max)	0.8 - 36	2.5	QFN10 (3x3)
MP2467	500KHz (Fixed)	6 - 40 (Max)	0.8 - 30	2.5	SOIC8E
MP4461	4MHz (Adj.)	4.5 - 40 (Max)	0.8 - 36	3.5	QFN10 (3x3)

Efficiency vs Load Current



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Globally, engineers share similar gratification and concern pg 61

Reference designs worldwide: understanding the IP imbalance pg 75

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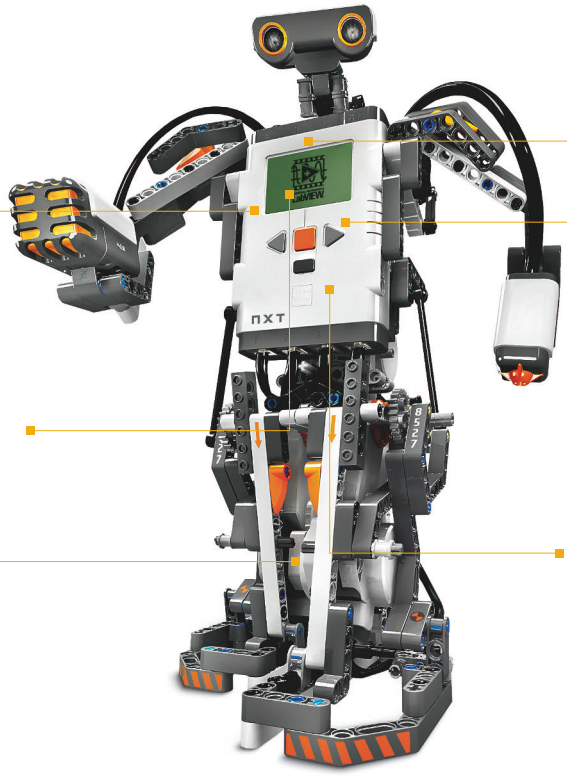

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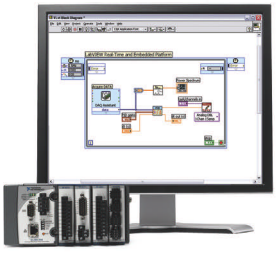

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Globally, engineers share similar gratification and concern

BY MAURY WRIGHT • EDITORIAL DIRECTOR, *EDN* WORLDWIDE

"It was the best of times. It was the worst of times." The classic Charles Dickens quotation could easily have applied to the situation in the engineering profession last year. Engineers are worrying about outsourcing of their jobs, feeling decidedly underappreciated, and working what they believe are excessive hours. But engineers receive higher compensation than workers in many other professions, and job satisfaction is high. This conundrum led *EDN* to conduct its first salary-and-career survey, and we believe it is the only such survey ever fielded worldwide. A summary presentation of the results here kicks off our fourth annual *Global Report*, and, as in the past, the print offering is a small part of the complete online *Global Report*, which you can find at www.edn.com/global.

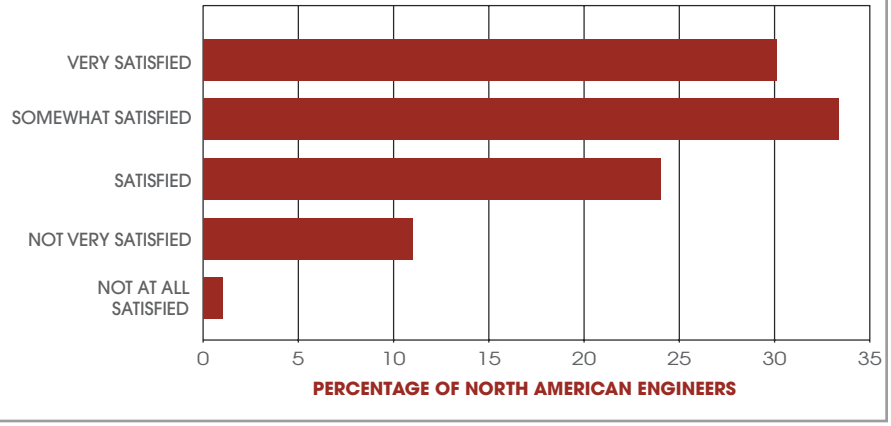
Over the summer, *EDN* and our regional global editions conducted the salary-and-career-satisfaction survey. *EDN* in the United States focused on North America, *EDN Europe* focused on Western Europe, *EDN Japan* focused on Japan, and *EDN China* focused on mainland China. *EDN Asia* fielded surveys separately in India, Korea, Southeast Asia, and Taiwan. We conducted the surveys via e-mail. We are hosting the complete set of data that we gathered in a new career section of our Web site. On the Web, you will find the intricate details on how we fielded the surveys as well as all of the data. Here, we'll take a look at details that stand out along with some of the most interesting verbatim responses that we gathered.

JOB SATISFACTION

The combination of outsourcing and staff reductions has left North American engineers worrying about their future. Meanwhile, new engineering opportunities abound in parts of Asia. The situation seems ripe for a vastly different set of results when you ask engineers globally how satisfied they are with their career. And you might expect poor job satisfaction in North America.

Figure 1 shows the results from North America. Surprisingly, most respondents in North America feel somewhat satisfied to very satisfied. The 30% that chose very satisfied dwarfs the response in that category from all of the regions that *EDN Asia* covers. We admit one slight discrepancy. Arguably, we incorrectly ordered the "satisfied" and "somewhat satisfied" choices on the questionnaire, but that

FIGURE 1

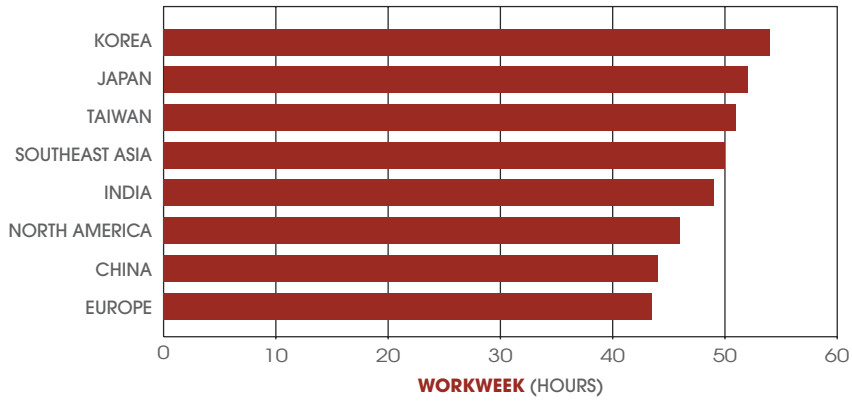


discrepancy certainly doesn't affect the "very satisfied" category. Check the online details, and you will see that only India came close to North America at 27.2%. Europe also delivered positive numbers, and the **sidebar** "UK engineers relish working with technology and quality of life" chronicles several such engineers. Conversely, in Japan, only 2.8% feel very satisfied. Excluding North America, the job-satisfaction curve has the traditional bell shape.

Looking at verbatim responses from engineers in North America, it's hard to match those responses to the **figure**. There are plenty of positive responses, but there are also plenty of negative ones.

Outsourcing is near the top of the list of complaints. One North American respondent noted as a concern, "Job security—my company generally takes attrition in the US and does massive hiring in China and India. I'm even hearing of start-up companies that want to outsource all product development to India or China to conserve capital." Outsourcing isn't just prevalent in North America. Japanese respondents indicated that 18.7% of their design work is outsourced.

FIGURE 2



CHINESE EEs SEEK TRANSFORMATION BEFORE THE AGE OF 35

Jeff Lu, Executive Editor, EDN China

China's electronics industry has grown rapidly in the past two decades. The growth is a key reason than many young Chinese select electronic engineering as their occupation. In the past decade, China has transformed beyond its role as the manufacturing center of the global electronics industry. As local OEMs have matured and more and more multinational companies have established R&D centers in China, the amount of design work has skyrocketed. Today, young Chinese electronic-design engineers get more job opportunities, better salaries, and loftier social status than engineers in other industries. Nonetheless, many young engineers are acutely concerned about continuing in a design job after the age of 35 and look toward management and entrepreneurial opportunities.

"I have been considering transformation," says Nathan Lei, project manager of a German communications company's Shenzhen office. Despite many years' work experience at UT Starcom and a master's degree in electronic engineering from Hong Kong Polytechnic University, he says he does not want to be an engineer for a lifetime.

Two reasons drive the midcareer designers away from engineering. First, R&D is an arduous job. Young engineers need to spend a lot of time and energy to meet challenges in their daily work and still stay abreast of the latest technology. Overtime is commonplace for Chinese electronics engineers. As they age, the engineers are less willing to endure such intensive work requirements. If an engineer has not landed in a team-leading position on the strength of his experience and capabilities by the age of 35 and is immersed in development work, he will inevitably feel competitive pressure from more energetic young people.

Opportunity is the second force that drives engineers to other jobs. Today, opportunities abound in China's fast-growing electronics industry. Many young engineers yearn to one day start a company of their own. Generally, engineers believe that pure R&D work–even at a multinational company–will restrict their horizons. Experience built from R&D work does not qualify an engineer to operate a company. Therefore, many young engineers take on sales and marketing as their choices for the postdesign step of career development. The engineers hope to gain more experience in business and corporate operations before turning 35.

Generally, engineers believe that pure R&D work–even at a multinational company–will restrict their horizons.

Chongjun Zhu currently serves as general manager of the new-business-development department in an independent design house for handset products in Shanghai, and he is one of the company's shareholders. "Just a year ago, I was staying up writing code," he says. He is satisfied with the fact that he turned from an engineer into a business executive before the age of 35. Zhu believes that, in China's electronics industry, a technology-type executive who knows how to do business has greater potential for growth and success than an engineer. He believes that his experiences as an engineer were just steppingstones in his career development.

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Still, in North America and Japan, the prevailing mood is positive. And the primary reasons seem to be the satisfaction of tackling difficult problems, learning challenging technologies, and creating useful products (see **sidebar** "Technology creations drive Japanese engineers"). The North American survey identified "technical challenge" and "feeling of accomplishment" as the top two factors influencing job satisfaction.

The feelings extend to the global engineering community. An Indian respondent said, "I have been able to put most of my knowledge and skills in engineering to productive use. As I have worked in very small companies, mostly start-ups, I have been extremely hands-on and see the companies grow very visibly, and that has given me the most satisfaction."

A respondent from Europe noted, "A multidisciplinary engineering career has got to be the most satisfying career; how else can you help mould the World whilst you learn how it works—magical!" An engineer in Taiwan added, "There is an opportunity to develop new products and to realize my professional expertise," and a respondent in Southeast Asia stated, "Work is challenging in a way that there's always new problems to solve." Only China had a decidedly different take on satisfaction, choosing "advancement opportunities" and "benefits" as the two most important factors.

As for the most difficult challenge in their current jobs, Japanese engineers

UK ENGINEERS RELISH WORKING WITH TECHNOLOGY AND QUALITY OF LIFE

Graham Prophet, Editor In Chief, EDN Europe

Engineers in the United Kingdom have long had a complex relationship with their chosen profession. In almost any era of recent history, the industry has complained that it could not find enough engineers with the right skills. At the same time, engineers have frequently regarded themselves as under-rewarded in financial terms and undervalued in society relative to their contemporaries in other professions. As long ago as the late 1970s, this concern became so acute that the British government set up an official inquiry into the engineering profession. Industrialist Sir Montague "Monty" Finniston conducted this inquiry, which in 1979 proposed a number of remedies to enhance the status of engineers and increase the flow of aspiring young engineers into the profession.

To judge by many indicators in the UK engineering scene, not much has changed in nearly 30 years. You still hear many of the same gripes. So, are the UK's electronics designers an embittered and unhappy group? On the contrary, as a group, they seem to be happy with their chosen path.

A relatively recent entrant into the UK's engineering community is hardware engineer Charlotte Doyle, who designs embedded-system-computer boards for Varisys, a UK-based supplier of COTS (commercial-off-the-shelf) and custom hardware for the embedded-computer market. Having worked in the industry for five years since graduating from university in 2002, Doyle says, engineering has been the right choice for her. She is happy with the position she holds and says that electronic design, with its problem-solving challenges, continues to hold her interest, as someone who came into the profession through enjoyment of the technology. Her job, she says, also offers the right combination of conditions and benefits, and the company she works for is "family-friendly"–a theme that recurs in talking to today's UK engineering community. Within her field, she does not find that keeping up with technology is a particular issue. "There is time to keep up to date technically, as part of the problem-solving," she says. Doyle would see an ideal career path as one that allowed her to stay in engineering, "perhaps more involved with project management," but she has no wish to move into, for example, a sales or FAE (field-application-engineering) role.

When Doyle completed her university studies, financial institutions were trying to tempt engineering and science graduates away from technology and toward finance. The financial businesses told the recent graduates that the rigor of their scientific education would lend itself to this alternative career. "A number of people from my year group did that," Doyle says, "and they currently have significantly better rewards than those of us who continued with engineering." But she has no doubt that technology–and the engineering profession–has been the right choice for her.

Martin O'Hara is technical director at Danfoss Randall Ltd, leading a team of 15 designers of systems for heating controls. With a career that has included posts with Ferranti, Newport Components (now C&D Technologies), and Motorola, O'Hara is an example of an engineer who has kept technology as the focus of his professional life. The rewards of the job, he says, have shifted throughout his career from the fascination with technology itself to managing the process: getting a product through to production and interacting with teams in other geographically distributed branches of his company. Danfoss is a Danish company; other locations that O'Hara works with are in Slovenia and China.

O'Hara sees keeping up to date with technology as a significant challenge for himself and his team "in an environment of information overload." In material terms and perhaps due to a career structure in which he has always chosen a new area of technology with each move, O'Hara believes that he has fared at least comparably with and perhaps better than most of his peer group. He

continued on pg 66

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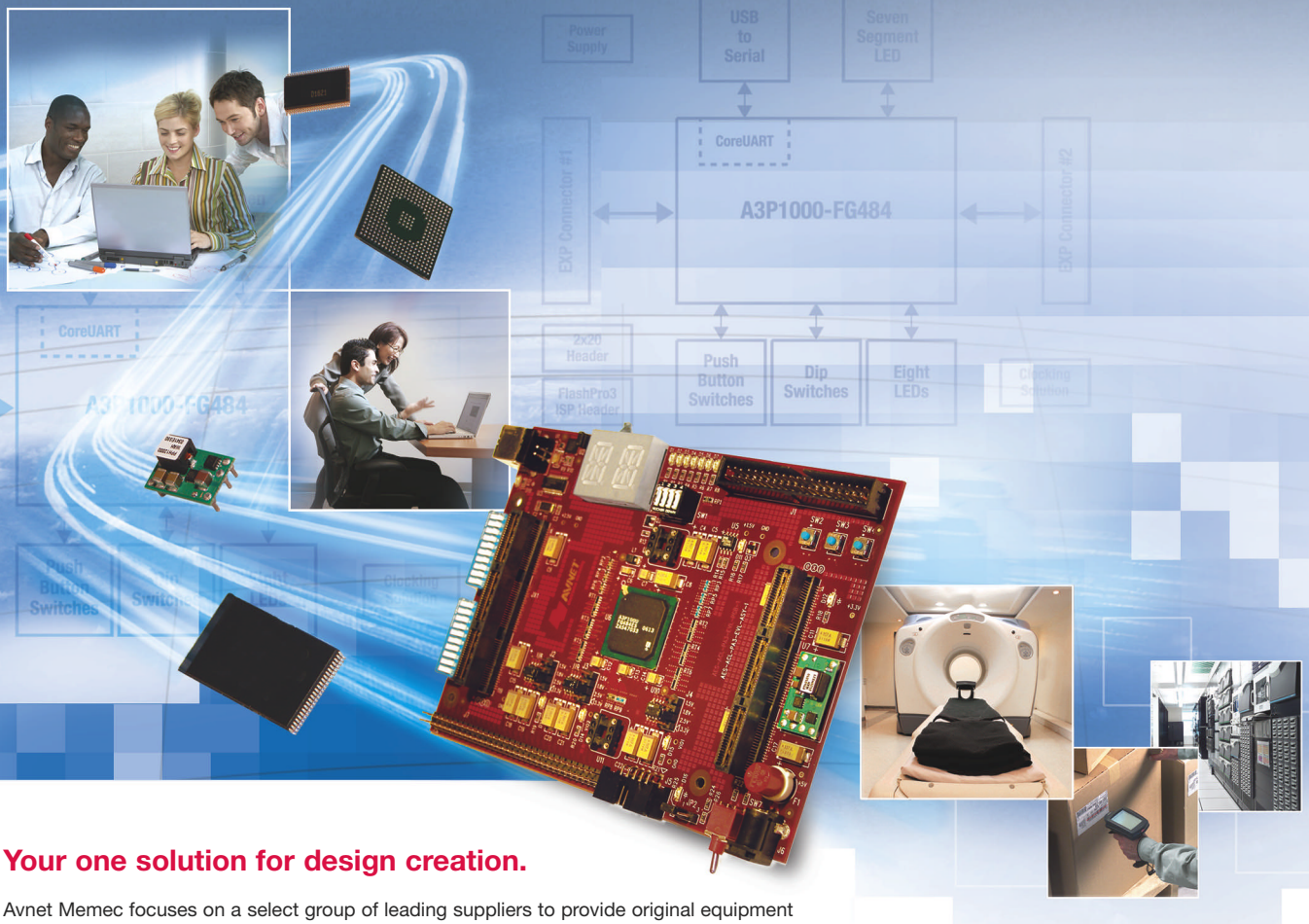

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yielded some surprising answers. They mentioned the expected time crunch, excessive workload, and technical challenges, but several responses mirrored one respondent's "shortage of midcareer engineers." On the other hand, the survey revealed an average age of 41.2 years, with an average of 15 years as an engineer and more than seven in the current job—presumably a midcareer description.

Several Japanese respondents also noted managerial issues. One respondent claimed a "divergence in consciousness with management" and another noted "arguing with the management team." Rightfully or wrongfully, many view Japan as a region in which engineers once wouldn't question authority, but that's not the case today. Old generalizations would also suggest that motivation would never be an issue in discipline-centric Japan, yet respondents identified issues with lack of motivation.

Without question, engineers globally feel time-to-market pressure and note the inevitably compressed schedules that are exacerbated by increasingly more complex technology. With regard to such challenges, an engineer from Southeast Asia pointed to "customer product deadline and debugging the complex boards." Responses concerning keeping up with technology were among the most popular among North American respondents. One noted "keeping on top of the current technologies" as the biggest

continued from pg 64

is also in a minority among UK engineers and engineering managers, in having added to his technological qualifications by earning a degree in management.

From a manager's perspective, O'Hara sees one of the UK industry's problems as a failure to attract sufficient young entrants to the profession. "In response to one of our recent advertisements, which was not specific on experience expected, no young graduates applied at all. All of the applicants were in the 35-to-45 age range," he says.

O'Hara values the freedom his current position offers him to "do what needs to be done" without excessive pressure on spending. There is also no great pressure on him to outsource design work, although he does contract out some work–mainly software.

O'Hara says it is becoming more difficult to find engineers with cross-discipline knowledge–for example, analog and digital or hardware and software–or designers with application knowledge. Although he does not outsource design, O'Hara notes a negative trend emerging with the general move to offshore manufacturing. "Without the link to manufacturing," he says, "the design community is losing design-for-manufacturing skills."

The ultimate expression of a wish to move your career progression ahead is, of course, to look for a new job. One person who sees that process in action is Kay Alexander, divisional manager of John Prodger Recruitment, a UK-based agency that operates across the breadth of the UK electronics industry. When British engineers seek a move, Alexander says, it's rarely just for financial reasons; more often, it's about moving their careers forward. She confirms that most UK engineers were initially attracted to the profession by their enthusiasm for the technology, and most would prefer a career path that keeps them in direct contact with engineering and that continues to present technical challenges.

Because of the lure of technology, most engineers prefer an upward move into engineering management rather than, for example, a move to sales or marketing. Ultimately, as Alexander points out, "A company needs only one chief technology officer." In cases in which engineers do leave a mainstream career path–what Alexander describes as "leakage" to the profession–it's most often to free-lance design work or into teaching; science teachers are in short supply in Britain's schools.

Alexander sees a trend in the increasing determination of engineers to consider family-friendly and quality-of-life factors, such as working hours, flexible working time, and paternity leave–as well as maternity leave, which is a legal right in the United Kingdom as in most other European countries–alongside direct career issues, such as pay and technological challenges. "A few years ago, these 'soft' topics would have been mentioned only late in a job negotiation," says Alexander. "Now, they are discussed right away. I think many companies have underestimated the contribution these factors can make to recruiting good people. It has become acceptable for engineers to put a high priority on these matters, whereas before it was not."

O'Hara agrees with Alexander's assessment and adds that, as his current employer is a branch of a Danish company, its engineers do enjoy favorable conditions in that respect; Scandinavian countries and companies are noted for progressive policies.

It is more difficult as a UK engineer to build a career in engineering and make a lot of money. An engineer with a few years' experience might earn less than £30,000. Alexander observes a problem with experienced engineers: "Eight to 10 years ago [at the height of the dot-com 'bubble'], a lot of engineers moved from, for example, defense into communications, which was relatively much better paid at the time. Now, there is interesting work opening up in defense and other areas. Companies need those experienced engineers but cannot pay enough to tempt that cadre of engineers out of their current positions."

It is becoming more difficult to find engineers with cross-discipline knowledge–for example, analog and digital or hardware and software–or designers with application knowledge.

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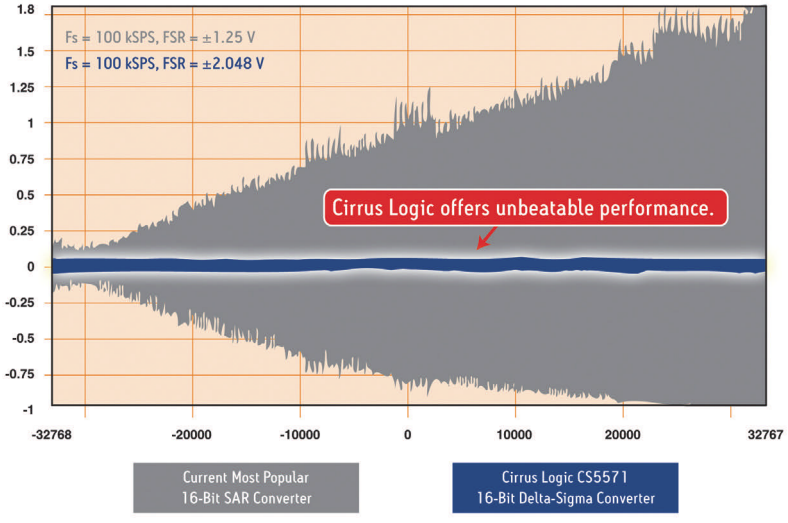

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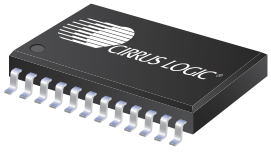
CS5580	16 bits	200 kSPS	0.1LSB	1, Differential	70 mW
CS5581	16 bits	200 kSPS	0.1LSB	1, Single-ended	70 mW



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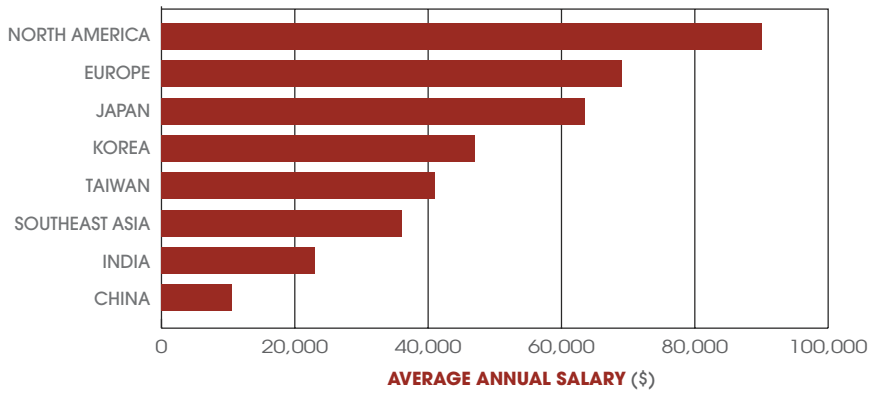
challenge. "[I] finished college over 15 years ago, technological advances are happening all the time, and keeping abreast of the latest and greatest is time-consuming in itself."

FIGURE 3



LONG DAYS, LONG WEEKS

Complexities of enabling technologies and end applications combine with tight schedules to make workload a global problem that straddles the issues of job challenges and job dissatisfaction. We asked engineers about the number of hours that they work per week. **Figure 2** summarizes the results; the hours they work range from 43.5 to 54 per week. The gap of more than 10 hours seems small, but it represents approximately 25% of the workweek. If you peruse the online data, you will find wide ranges of responses in each region. In Japan, for instance, more than 10% of the respondents work more than 60 hours per week.

Verbatim responses and other data indicate a more trying workload situation than **Figure 2** depicts. The **sidebar** "Korean engineers face mandated career choices" paints the profession as a 365-day-a-year job in that region. A North American respondent chose "work-life balance" as a key challenge, adding, "My employer is always wanting more of my time than I can give and then downgrades my performance because I cannot give as many hours as others." A number of Taiwanese respondents note overtime work as an issue, especially relative to their pay.

JOB DISSATISFACTION

Other factors in job dissatisfaction range from complaints about management to lack of recognition and decision-making power. Japanese engineers' sources of job dissatisfaction match those in other regions, but responses that stood out relate to career track, skills, and decision-making. One respondent noted, "My technical capabilities are too narrow." Several mentioned the gap between the job at hand and the job that they would prefer to perform. Perhaps the most notable response, however, is "not authorized to make a decision." Engineers globally believe in their ability to do their job and make good decisions, and Japan has among the deepest of experienced-talent pools.

Career track appears to be a big issue in China. According to the **sidebar** "Chinese EEs seek transformation before the age of 35," Chinese engineers seek to move into marketing or sales roles by midcareer. Some Korean engineers, on the other hand, would prefer to stay on a technical career path but are forced into management.

The engineering profession in other parts of Asia is far younger both figuratively and literally than in Japan. That fact translates to lower pay, less job choice, and, potentially, greater dissatisfaction.

Responding to the dissatisfaction question, an Indian engineer from our *EDN Asia* survey noted, "I'm dissatisfied because of the pay structure of my company. I am still not into a proper development project. I'm forced to take on the assignments mandated by management. My achievements are not recognized."

But the positive responses in India outnumber the negative. Remembering that India is a newcomer in prevalent relatively-well-paying engineering jobs, it's still humbling to read a reason behind job satisfaction such as "sense of accomplishment and, of course, money for bread."

Not surprisingly, making a living and salary top the list of concerns for engineers globally. Our survey has a lot of

TECHNOLOGY CREATIONS DRIVE JAPANESE ENGINEERS

Takatsuna Mamoto, Editor in Chief, EDN Japan

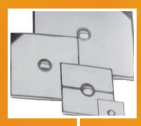
A couple of trends are evident in the career choices of Japanese engineers: They yearn to create and build things, and the skills that their fathers and mentors possessed influence them. "Watching my father make things during my childhood led me to an engineering career," says one. Another notes that, when he was young, his father's skill in repairing broken radios, TVs, and VCRs impressed him.

The creative instinct provides the biggest motivation. "It is always nice to see that the product I design is a bestseller," says another Japanese engineer.

"I am satisfied to be involved with development of the state-of-the-art robots that walk on two legs," says still another. "It was my childhood dream."

The engineers also greatly appreciate and are proud of the recognition that they receive, especially when trade publications cover the technologies and products on which they work.

Japanese engineers are generally happy with their career choices. Some note the difficulty of long hours and lengthy product-development schedules. Others note the occasional mismatch of skills on a design team to an application. But the sense of accomplishment the engineers feel after developing a successful product makes the work worthwhile.

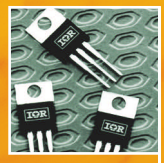


1947: IR opens for business, launching selenium rectifiers

1954: Commercializes germanium rectifiers

1959: A pioneer in silicon controlled rectifier (SCR)

1962: Introduces new epitaxial process for producing industry's most stable high voltage SCRs



1979: Patents first commercially viable Power MOSFET (HEXFET®)

1980: Introduces high reliability power semiconductor devices for space programs

1983: Launches first commercially viable high voltage power ICs

1996: Introduces MOSFET and Schottky in a single package

1950 **1960** **1970** **1980** **1990**

2000

Introduces wafer level package (FlipFET™)

2001: Invents integrated building blocks for DC-DC converters (iPOWIR™)

2002: Introduces integrated design platform for motion control (iMOTION™)

Invents first dual-sided surface mount package (DirectFET™)

Invents scalable multi-phase architecture for DC-DC buck conversion (xPHASE™)

2003: Introduces iMOTION™ Digital control ICs

2004: Sets new standard In lighting ICs

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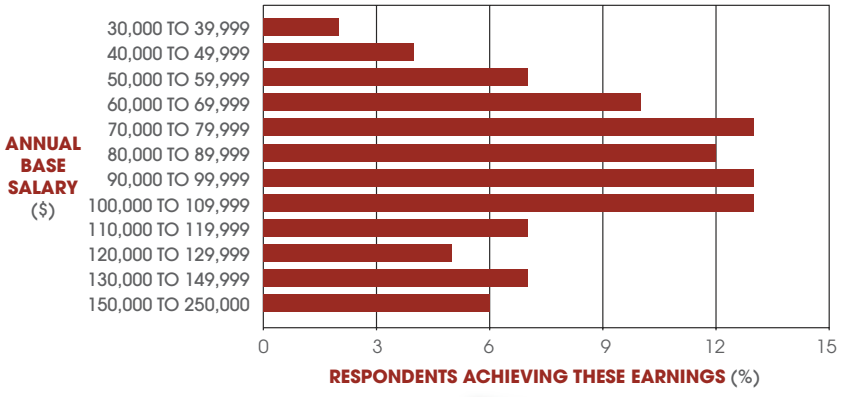
data on salaries, and you should explore the Web data for details. The highlights follow.

First, we offer a disclaimer. We conducted all of the surveys with salary questions pegged to local currency. We then converted the amounts to US dollars. The conversions were accurate in August 2007 when we compiled the data but will vary—possibly greatly—over the long and even short term.

North American engineers won't like a quick generalization of the results in Fig-

FIGURE 4



KOREAN ENGINEERS FACE MANDATED CAREER CHOICES

Jade Jin, Executive Editor, EDN Korea

Since 1990, the electronics industry has driven economic growth in Korea and has become one of the chief national industries. Accompanying the industry growth, an increasing number of engineering opportunities have emerged. The engineers largely like the profession, although some feel they have too little choice about how their career progresses.

For example, Senior Engineer Kyung-Fan Shin at the Overseas HSDPA (high-speed-downlink-packet-access) Development Group of Pantech and Chief Engineer David Yoon at the Mobile Communication Lab of LG Electronics both majored in electronics engineering in the early 1990s. Both have also worked since 1996 as engineers in the telecommunication field in Korea, which has experienced the rapid growth of the electronics industry. Moreover, the two have worked as engineers in mobile communications and directly on mobile handsets. More than any other segment, mobile communications has been the heart of the Korean electronics industry for more than 10 years.

Generally, engineers sacrifice their personal life in Korea to survive in the competitive field. Work that continues for 365 days a year and frequent overtime hours are the symbols of the profession. Given those facts, you might expect this duo to complain about such conditions, but generally they like their jobs.

"Engineering is a realistic and creative occupation," says Yoon, who develops GSM (global-system-for-mobile)-communication and WCDMA (wide-code-division-multiple-access) mobile phones at LG Electronics after working for the Wireless Telecommunication Division of Samsung Electronics. "When the products I develop are used in everyday life and the end users are satisfied with them, I feel joy as an engineer." However, he notes, "As the lifetime of products is getting shorter, I have been under stress due to the pressure for shorter development cycles and excessive work hours. But I have the greatest sense of accomplishment when I acquire command of new technologies and resolve problems."

"Engineers design the world by exploring new areas and leading technologies," says Shin. "So, Korea has to accommodate the trends of the global market as well as the Korean market and should make efforts to continue to do self-development. These requirements represent the pride and pressure of engineers."

The demand that engineers move beyond design jobs proves to be the biggest complaint of Korean engineers. "I envy engineers who have worked in foreign countries for 30 to 40 years," says Yoon. "It is difficult to be an engineer for more than 10 years in Korea. In most cases, engineers are promoted to engineering management in accordance with a promotion system. Because personal choice is not allowed, the prospect of working in an engineering role throughout a career is not guaranteed."

"When the products I develop are used in everyday life and the end users are satisfied with them, I feel joy as an engineer."

The engineers identified mobile phones and mobile communication as technologies on which Korea should continue to focus. Global standards are now incorporated in 4G technologies that Korean companies developed. Accordingly, Korea should lead in 4G technology and have a competitive edge when the market accelerates.

Other strengths include robotics. "We should focus on robot technologies in the long haul," says Shin. "The trends of technologies will change from mobile phones to robots at home and overseas. The robot technologies are applicable to a variety of fields, such as games, electric home appliances, and industries. Many Korean companies, including Pantech, are paying attention to the technologies or are now developing them."

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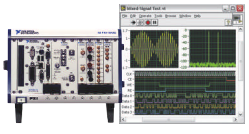

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ure 3. That data—touting a $90,000 annual average salary—screams "North American engineers are overpaid." The inequity between average salaries in North America and those in new engineering markets, such as China and India, will surprise few engineers. Moreover, engineers in those regions generally benefit from a very low cost of living. But engineers in mature markets, such as Japan and Europe, trail North American engineers by a broad margin, as well. And the cost of living in parts of Japan and Europe is higher than the cost of living in much of North America.

A more detailed look at the full compensation charts that we present on the Web paints a bit of a different picture. For instance, 13% of North American engineers make $90,000 to $100,000. In Japan, 9.8% make roughly $84,000 to $101,000. Moreover, the bulk of the Japanese engineers are clustered in groups making slightly less than $84,000. A look at the salaries above and below the average North American salary does not suggest an almost $27,000 gap.

The big difference in North American and Japanese salary distribution really comes at the high end of the range. **Figure 4** shows that 6% of the engineers in North America make more than $150,000. Check the Web, and you will see that the percentage of such earners in Japan is approximately 0.5%.

In North America, engineers have surely benefited from stock options and other forms of bonuses that boost salary. That compensation could partially explain the difference. Again, however, close perusal of the online data provides more hints. In the North American survey, a greater number of respondents are in the R&D and engineering-management categories than those from Japan, whereas the Japanese survey has a greater percentage of design-engineering respondents. The European responses fall between the North American and Japanese responses, with 3% earning more than $150,000 and a relatively high management response.

There is no way to rationalize the gap in other regions, other than to accept that engineering salaries across Asia, except Japan, significantly trail North American salaries. The facts are that $90,000 salaries are simply unheard of in the regions that *EDN Asia* surveyed.

FIGURE 5

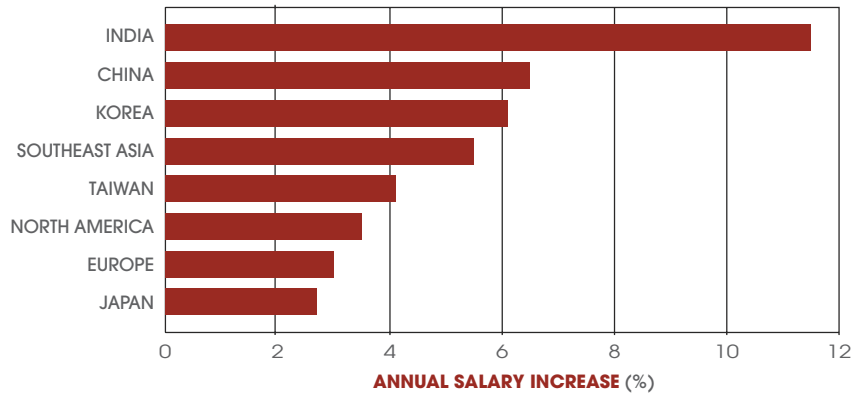
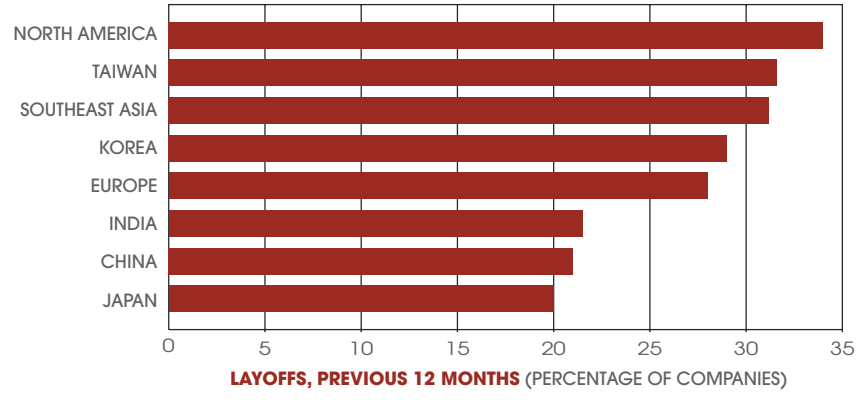


FIGURE 6



RAISES

The good news for engineers across Asia is that the gap will close as engineers from India to Korea are getting greater annual increases percentagewise than Japanese and North American engineers. A number of verbatim responses lament low pay and nonexistent or small raises. One respondent from Taiwan stated, "There have been no increments in salary for a long time. In the long run, my salary might even be reduced."

Overall, however, our survey paints a brighter picture. **Figure 5** shows the annual average increase by percentage. India tops the list at 11.5%, but even the typical average increases across Asia come in at approximately double the average increases in Europe, Japan, and North America. In India, more than 30% of workers received a 10 to 20% raise.

STAFF REDUCTIONS

We asked the respondents in every region whether their companies had laid off engineers in the previous 12 months. **Figure 6** depicts the results. Frankly, the results are pretty good. Most companies lay off some number of workers, either to eliminate employees that aren't superstars yet aren't performing poorly enough to fire or to scrap one project at the expense of a competing project.

We also asked respondents whether their companies had hired engineers in the previous 12 months. The answers were uniformly positive, with India at 93.6% and North America at 73%. Of course, we asked the respondents only whether their companies had hired engineers in the previous 12 months—not where the jobs were located. To relieve those of you in North America worrying that the new jobs were overseas, 89% of the North American respondents revealed that the jobs were indeed located in North America. EDN

You can reach Editorial Director Maury Wright at 1-858-748-6785 and mgwright@edn.com.

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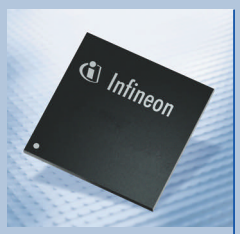

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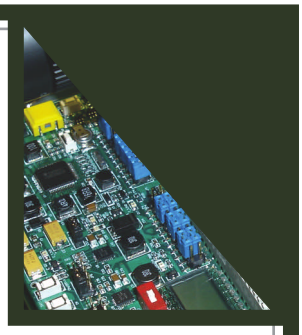


Reference designs WORLDWIDE: UNDERSTANDING THE IP IMBALANCE

BY NICHOLAS CRAVOTTA • CONTRIBUTING TECHNICAL EDITOR

With the rising complexity of silicon and software design, it has become critical for component vendors to supply more information than just a data sheet to get engineers started on their designs. Reference designs are important ways for companies to pass on IP (intellectual property) relevant to the effective use of their products. The term "reference design" itself is a fairly ambiguous term and can even take on different meanings within the same silicon company (see **sidebar** "Defining reference design" at the Web edition of this *Global Report* at www.edn.com/global). For example, a company's FAEs (field-application engineers) serving North America may use the term to refer to a paper schematic or an evaluation board with limited application software. FAEs from the same company working in Asia, however, may use the term to refer to a fully designed product, perhaps missing external plastics, that is ready for mass production (see **sidebar** "MTK pioneers complete designs and garners de facto monopoly in handsets," also at www.edn.com/global).

Some companies claim that they create reference designs to demonstrate their expertise and market leadership. The reality is that reference designs are all about selling components used in the design. Reference designs require significant expense to create, and this expense limits the number of designs that any company can offer.

How countries around the world use reference designs directly influences which ones a company will create and, more important, how they will use them to generate design wins. Component vendors make deliberate decisions about where they target their reference designs, thus placing engineers in different countries in competition with each other in a way that directly impacts their access to a vendor's engineering and support resources. In other words, the uneven flow of IP is changing the global engineering landscape.

GLOBAL TRENDS

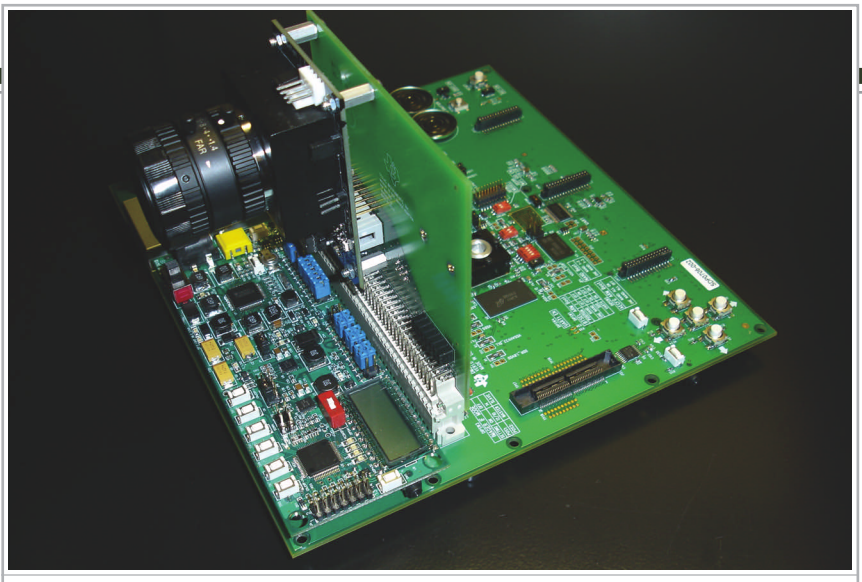
It's difficult to track trends for the use of reference designs in regions of the world. After all, it's a fine line between describing a trend and perpetuating a stereotype. How a company approaches the acquisition of IP depends greatly upon its size, maturity, region, and culture. For example, China, with its lower cost of labor, focuses more on the BOM (bill-of-materials) charges than on the NRE (nonrecurring-engineering) charges. The opposite situation can be true in North America, where engineers are willing to program in C to save design time but at the expense of a larger program memory and a higher performance, more expensive processor. Across Asia, companies

are open to reference IP from IP cores for chip design to complete system designs. Speed in bringing just enough features to market is key (see **sidebar** "Reference designs: What separates Asia from the rest?" at www.edn.com/global).

It's always dangerous to generalize, but if you had to describe each country in only a few words, the following trends and stereotypes might suffice. For example, NIH (not-invented-here) companies, which those in North America typically are, have a great deal of internal experience on which to fall back. These engineers focus on one application in contrast to a component vendor's engineers, who develop application-specific IP for relatively unrelated designs from project to project. As such, the NIH engineers can produce optimal designs. Some reference materials are nice to have, especially for accounting for the obscure and frustrating nuances of a component, but they serve only as launching points for more sophisticated designs. This approach typically maximizes performance and the number of features but incurs the greatest investment and overhead.

In "after-the-fact" environments, such as Japan, engineers are also experienced and create superior products. However, they like to have comprehensive reference designs available not to build upon but to compare with their own designs. They like to work out all the details for themselves, which, like taking the time to solve a puzzle rather than looking at the answer, stretches their skills and improves their mastery of the technology (see **sidebar** "Japanese engineers focus on original designs and customization" at www.edn.com/global). They don't want to repeat what others have done, but they want to see how they've done it. The reference design acts as a final check, perhaps revealing only minor idiosyncrasies in component specs that the engineers overlooked.

The distributed-IP-design model, typical of the United Kingdom, focuses on IP management at the distributor level. European distributors typically add value and increase profits by providing not only chips, but also complete subsystems that designers can drop into a design with limited modifications. In effect, distributors act as IP brokers between component companies and OEMs. This approach can significantly impact component selection. Although NIH-focused engineers may resist such offerings, some distributors in North America are beginning to explore this approach. To learn about one European system house that always begins designing before reference-design availability, see **sidebar** "Getting to market first precludes a wait for a reference design" at www.edn.com/global.



A Texas Instruments digital-camera reference design comes complete with a camera lens and a sensor.

Some companies, such as those in Taiwan, take an "as-is" approach, taking reference designs mostly as the component vendors supply them. Their goal is minimal investment and fastest time to market. In some cases, an ODM (original-design manufacturer) stands between component vendors and OEMs. ODMs take on the burden of understanding an application market as well as related silicon, software, and system issues. ODMs work with component vendors to create their own reference designs, which they then sell to OEMs that want to quickly get to market. For example, an ODM may create a fairly complex digital-camera design. The ODM then sells this design to multiple OEMs, which personalize the design, perhaps by creating only the external plastics or introducing a differentiating feature, such as antishake or red-eye removal (see **sidebar** "Reference software" at www.edn.com/global).

In another environment, such as India, application engineers with little real-world experience don't always have the luxury of leisurely earning their expertise. Instead, they act as "sponges," learning on the job. In these environments, not making mistakes is critical for employment. These engineers consume reference designs, poring over boards and schematics, trying to soak up whatever knowledge they can while still producing designs as quickly as possible.

In contrast, the Chinese design environment is more of a "chop shop." The focus is on adapting reference designs for end products and minimizing costs. Reference designs by nature are somewhat generic so that you can apply the IP you capture in them across a wide range of applications. Reference designs drive sales of components, so the more customers who can use the design, the better. This approach recognizes that a reference design probably isn't as cost-effective as it could be and brings up images of an "engineer" ripping components off the reference board until it stops working and reducing it to its bare essentials. Swapping lower tolerance or alternative components is also common.

MARKETING BY EDUCATING

To increase sales, reference designs must meet the critical needs of engineers in education and reduction of overall design cycles (see **sidebar** "Pitfalls" at www.edn.com/global). For companies that don't care about adding their own IP or advanced features, time to market is everything (see **sidebar** "Reference designs open doors in Taiwan"). "The more of a turnkey design they can start with, the quicker they can realize product, though the Asia market is progressively becoming more self-sufficient," says Steve

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Marsh, strategic-marketing manager for the digital-signal-controller division at Microchip (www.microchip.com). "If we could do form factor, that would be even better for this subset of customers." A speedy, successful design is critical to the survival of these companies. "They want to be able to say that they've done a particular application so they can claim expertise with the technology to their next potential customer," says Marsh.

Even Korea is proving a fertile market for ready-for-market reference designs (see **sidebar** "Reference designs improve but don't always offer full performance" at www.edn.com/global). In addition, some reference-design creators don't exhaustively test their designs, limiting their usage.

System companies that lack expertise in certain key areas may take evaluation boards to production. This "design" methodology quickly produces results but provides little log-term gain or understanding of why the design works. Users can repeat the design but cannot easily build on it as they could have if they had taken the time to understand it. Countries with younger, less experienced engineers are beginning to recognize this fact. For example, India and China each want to be the design center of the world, with the fastest service

REFERENCE DESIGNS OPEN DOORS IN TAIWAN

Mike Pan, Taiwan Bureau Chief, EDN Asia

Given the complexity and cost of system-design challenges that R&D engineers are facing, IC vendors provide their customers with reference designs that reduce time to reaching volume production by enabling manufacturability. Simplifying the path toward production is especially important for the Taiwanese electronics industry, which excels at low-cost mass production. "It is impossible for us to use a chip in our system if it comes with no reference design," says Allen Su, a senior engineer at Powercom Co Ltd, a provider of power-protection products, such as solar-cell, solar-panel, and UPS (uninterruptible-power-supply) products.

Many sources, such as chip vendors, distributors, and VARs (value-added resellers), are available for reference design in the industry. But the robustness of reference designs varies from company to company. "Some provide us only a data sheet and associated rules used in designing PCBs [printed-circuit boards] based on the chip, while others offer a more complete solution," says Aren Chen, a supervisor of the R&D division at Vivitek Inc, a manufacturer of IP (Internet Protocol)-surveillance and multimedia-communication products, including network cameras, video servers, and recording software.

Both Su and Chen agree that reference designs from foreign companies are more general-purpose, targeting diverse customers. Both engineers report that they must make significant efforts to meet their application requirements if they want to adopt these designs. "Foreign IC vendors can probably do a customized reference design for their first-tier customers but not for everybody," says Su.

Chen also has experienced insufficient support by an international IC vendor. The company used such vendors for DSP sources but later found that it could not adapt the operating system with the selected DSP product and that the product was too costly. To address these problems, the company developed its own SOC (system on chip), which is an unusual approach among system makers in the Taiwanese market. In addition to improved performance, the SOC offers flexibility, according to Chen.

Both Su and Chen believe that products from local IC makers are more complete than offerings from foreign chip suppliers. The reason for this superiority could be that local IC vendors leverage a geographical advantage and learn precisely what their customers want. Moreover, the Taiwanese vendors offer competitive costs and speak the same native language.

To fill the gap with small to mid-sized system makers in Taiwan, foreign IC makers cooperate with local distributors or VARs to promote their products. Actel, for example, recently announced a reference design in Taiwan to enable intelligent system- and power-management implementations. "To better support our local customers, we had expended our sales network by working closely together with local distributors and VARs," says Rick Lain, the company's director of sales for the Asia-Pacific region. "We have three VARs in Taiwan to deliver more specific solutions based on our chip to its targeted customer."

Distributors are other active sources of reference designs. "The mindset of our development in reference design differs from that of IC vendors," points out TW Lin, vice president of R&D and the field-application-engineering department at Zenitron Corp, a distributor of semiconductor and electronic components. "Business is business. IC vendors' reference designs always focus on how to let their chip perform better. In contrast, our focus is on manufacturability." Sometimes, the company provides almost a prototype or board ready for mass production, according to Lin.

Reference designs from IC vendors, especially from foreign IC vendors, are not available for manufacturing, says Lin. "For example, if an IC vendor bases its chip on a six-layer PCB, then we have to convert it into a four-layer PCB and find cheaper replacements for other components on the board. Meanwhile, we also take care of issues such as EMI [electromagnetic interference], signal integrity, and other electronic characteristics," he says. "All we have done is assist our customers in reducing the cost and accelerating the time to market for their products."

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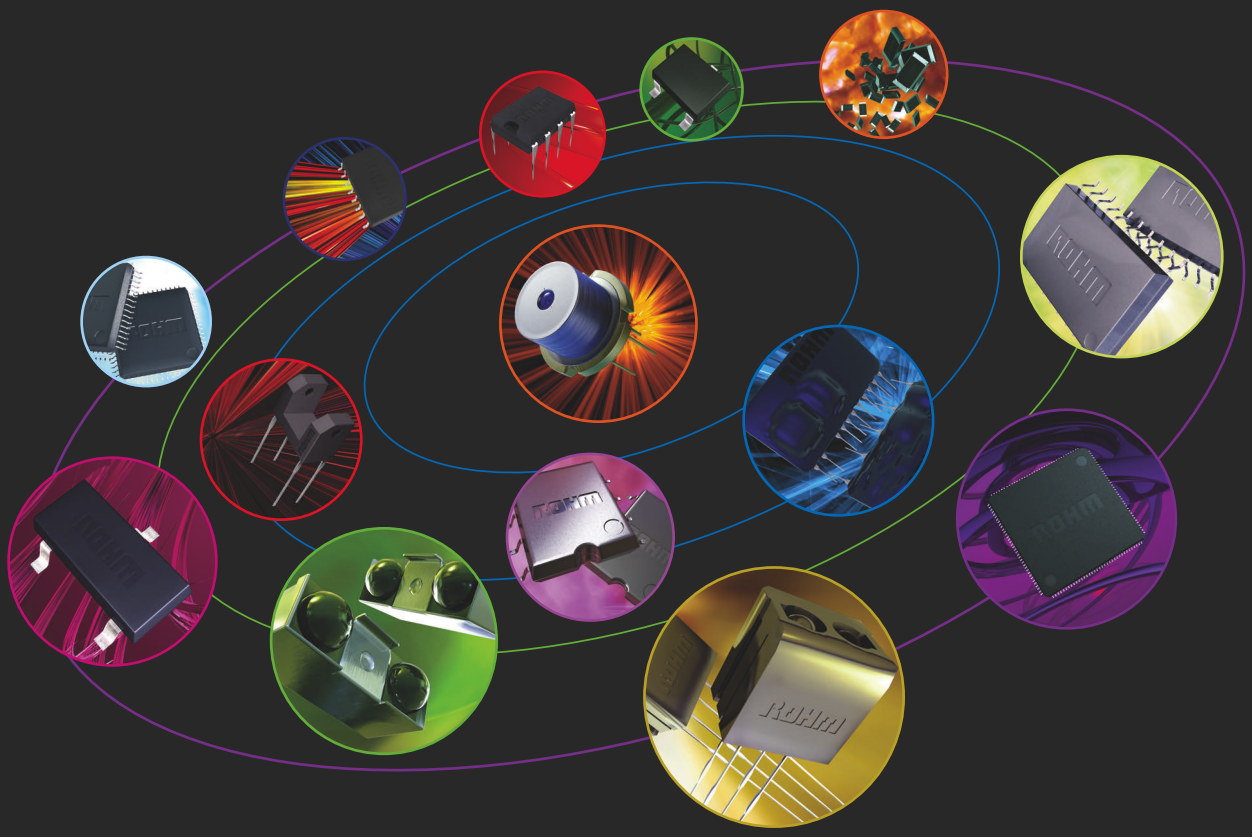

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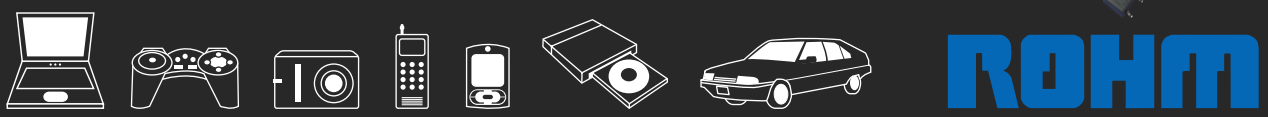

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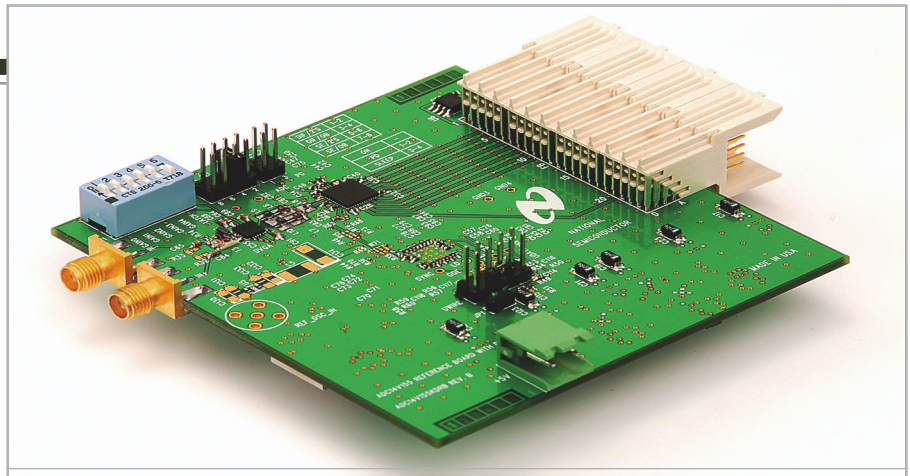

National Semiconductor's ADC14V155KDRB high-IF-receiver reference-design board enables immediate evaluation of a high-dynamic-range IF-sampling application.

and output. They continue to push for turnkey, black-box designs. They would be even happier if the form factor were also complete. But don't believe the stereotype that all they are doing is copying. These companies are soaking up information as fast as other companies can ship it to them.

India, for example, is experiencing tremendous growth. Estimates place the number of new engineering openings at 10,000 each year, which sounds like a lot until you consider that the pool of applicants competing for these positions exceeds 300,000. "Engineering offers young people a chance to escape the lower caste," says Rick Zarr, worldwide-technology-partnership-marketing manager at National Semiconductor (www.national.com), "and they rely heavily upon reference designs to fill the many gaps in their experience."

From this perspective, "engineering outsourcing" is a misnomer because engineering is more than just copying someone else's design. "Innovation, insight, and experience are hard things to export," says Zarr. "American culture is quite diversified, and this affects the way American engineers solve problems." However, in addition to learning the basics of engineering, these other countries are discovering what it takes to be innovative. They also understand that, if they do something well, they not only make a great deal of money, but also get the chance to do it again tomorrow.

The perception that the United States is a think tank and the rest of the world is the think tank's manufacturing arm is dangerously naïve, especially when you consider that the fully burdened cost of an engineer in North America is about $250,000, whereas that for an engineer in India with a master's degree in electrical engineering is about $45,000. Design houses in India are not shy about investing in the infrastructure and expertise they need to compete and aggressively leverage their salary advantage.

For component vendors, these inexperienced engineers represent a tremendous opportunity, which they can capitalize on through reference designs. Rather than teach how to solve problems using general concepts, which they can apply anywhere, they can teach problem solving using components. In other words, instead of showing an engineer how to lay a trace or hold impedance constant, they provide a Gerber file that supplies the necessary trace. The file teaches the engineer something about traces but perhaps not enough to give the engineer the confidence to bring in a different component. In such a case, components in a reference design are more than just suggestions or recommendations. They lead to design wins and direct sales.

Reference designs also cover for lack of distributor expertise. The more product lines distributors take on, the less time they have to learn about—and pitch—each part. Reference designs open the door to innovative ways of helping distributors effectively sell parts.

Some companies offer bevies of reference designs for downloading from their Web sites. The application-specific knowledge these resources share is also component-specific, so there is a value in working even with smaller design houses, because they are learning to use a subset of the components on the market. Engineers with a mandate to produce quickly tend to design with what they already know. Reference designs effectively seed this market.

Reference designs are not simply about showing engineers how to design around a component, such as a processor. In fact, for secondary-component vendors, reference designs can be their most powerful marketing tools. Consider a company evaluating a digital chip that has little idea of how to implement any associated analog circuits. If it selects the digital chip, the company will most likely also go with the secondary components in a reference design that makes up the analog support circuitry. The same situation applies to RF subsystems, power supplies, assembly-level algorithms, and whatever other expertise a company lacks.

Many component vendors leverage associated design wins through cobranding with noncompetitive suppliers. Jointly developing a reference design reduces investment cost and increases the overall exposure of a design because multiple companies and distributors distribute the reference design. Also, cobranding increases the number of reference designs a company is associated with, a factor that some companies believe indicates market leadership. Partnerships can range from developing application notes together to creating whole portions of a production-ready design.

UK distributors execute another form of cobranding by combining suppliers to create reference designs. "Distributors are looking for ways to increase profits by adding value beyond simply supplying components," says Alan Hutton, partnership manager for Europe at National Semiconductor. "More and more, they are accomplishing this by providing complete subsystems."

Selling systems through cobranding has many advantages. First, it spreads the investment of creating the reference design among several vendors. Second, it enables vendors to highlight features that their customers may not understand well. For example, a design may benefit from implementing dynamic-voltage scaling on the main processor. Because a relatively inexpensive microcontroller manages scaling, it may seem more complicated to implement than it is to someone unfamiliar with the technology. By

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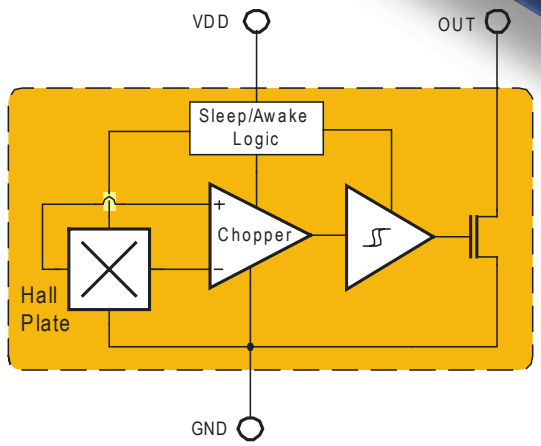
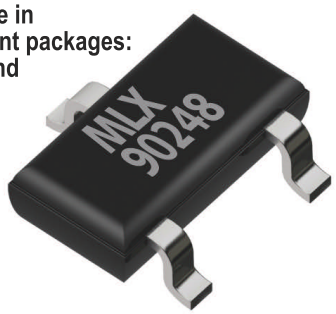


The MLX90248 is available in 2 ultra-small surface mount packages: The 6-pin (LD) package and the 3-pin (SE) package.



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having the scaling as part of the reference design, an engineer can experiment with it firsthand and see its potential benefits. Additionally, the implementation may reveal useful "best practices" or show how to reduce the number of required front-end components.

If the engineer likes the feature, the processor vendor wins because this factor may help lead the customer to select this component. At worst, another customer gets educated on the technology behind the feature. And the engineer can implement the feature with no additional design expense because it is possible to just lift the dynamic-voltage-scaling circuit straight from the reference design.

This win is key for the other vendors involved in creating the reference design because it helps tie secondary components to the selection of a primary component. It becomes a system sale rather than a tool sale of a single component, which distributors like because they can sell several parts at once. Although an engineer could select the main processor and choose different components to implement dynamic-voltage scaling, it is tempting just to take the entire subsystem because someone else has specified all the components.

Component vendors or distributors sometimes team up with local design houses to create region-specific reference designs. For example, these vendors and distributors will use regional vendors as sources for secondary components on a board. If the secondary components come from a foreign or more expensive source, this approach significantly reduces the value of the reference design. The effectiveness of cobranding in China, India, and the United Kingdom, however, can have a negative impact for other countries. When China and India ask for reference designs, they purchase components. The NIH attitude of requiring a reference design just to look at a part and not necessarily buy it yields fewer returns. Additionally, because NIH engineers tend to trust their own designs more than those from component vendors, the sale of secondary components is less certain. Ideally, these engineers don't want to depend on reference designs.

As a result, cobranding tends to be more effective in China and India, prompting companies to focus their efforts at those companies from which they get a better return. This factor potentially impacts worldwide engineering outsourcing. As more design decisions and sales move offshore, so does a company's focus of its limited design resources. To some degree, the refusal of NIH engineers to demand and use more comprehensive reference materials leads to a shrinking willingness of component companies to provide them any.

THE KNOWLEDGE GAP

The competitive edge that engineers gain from specialized knowledge is shrinking and will continue to do so for many mainstream applications. Reference designs that supply basic hardware and software functions make it possible for smaller players to enter markets with a relatively small up-front investment.

COBRANDING TENDS TO BE MORE EFFECTIVE IN CHINA AND INDIA.

"Reference designs, especially software algorithms and libraries in our case, are key enablers to help accelerate product time to market," says Richard Fischer, applications-engineering manager for the digital-signal-controller division of Microchip. "If we provide a complex algorithm, either for a vertical application or for a horizontal technology, this gives us a broader base of customers for our processors."

Providing more of the overall design or subsystem continues to play an ever-growing role in selling silicon. "It's one thing to say what a customer should achieve as it relates to performance; it's another to actually walk in the shoes of the customer by designing a complete system and realizing that performance for yourself," says Kanika Carver, digital-imaging marketing manager at Texas Instruments (www.ti.com). "These system-level designs are much more complex than first imagined, requiring system-level IP versus components. The more we provide of the complete solution, the more we learn, and the more effective the silicon and software we can offer."

Differentiation, therefore, no longer focuses on the product level, but on the functional level. Differentiation continues to refine, narrowing down to specialized feature support or extreme cost cutting. In this way, reference designs also narrow the gap between mature companies, which focus on developing most of their own technology, and aggressively agile companies, which focus on carving away a small portion of large markets for themselves.

Reference designs enable more companies to work with complex technology and create viable products. It's not that IP is disappearing from those that possess it but rather that it is trickling down faster than it ever has before. Not everyone is thrilled about the increase in shared IP. For example, a GPS (global-positioning-system)-module manufacturer has made significant investment in developing designs. Understandably, the company may be unhappy when an RF-silicon vendor wants to further educate its customers with a production-ready reference design.

This prospect can be either exciting or disturbing. India is hungry and learning fast, and everyone wonders what impact that thirst for knowledge will have on the engineering establishment, because the power in a technocracy is based on limited access to knowledge. A major shift is in progress, with countries such as India working to acquire expertise and the ability to provide quality comparable with that from other countries.

For all the talk about a global economy, most companies still focus primarily on preserving their own pieces of the market pie. Is an equal distribution of engineering expertise good for the world, for each country, or for a particular company? Outsourcing has long been a volatile topic. Is it possible for India to pull itself up the technology ladder without pulling someone else down? Electronic design continues to become more complicated, and the number of layers of companies involved in a design continues to increase. There is room for more players in the design process than ever before. And, given the size and the myriad distinct demands of the global market, there is also more room to specialize. EDN

You can reach Contributing Technical Editor Nicholas Cravotta at editor@nicholascravotta.com.

LINEAR TECHNOLOGY

DESIGN NOTES

Tiny Synchronous Step-Up Converter Starts Up at 700mV

Design Note 428

Dave Salerno

Introduction

Alkaline batteries are convenient because they're easy to find and relatively inexpensive, making them the power source of choice for portable instruments and devices used for outdoor recreation. Their long shelf life also makes them an excellent choice for emergency equipment that may see infrequent use but must be ready to go on a moment's notice. It is important that the DC/DC converters in portable devices operate over the widest possible battery voltage range to extend battery run time, and thus save the user from frequent battery replacement.

Single-cell alkaline batteries, with a 1.6V to 0.9V range, present a special challenge to DC/DC converters because of their low voltage and the fact that their internal resistance increases as the battery discharges. Thus, a DC/DC converter that can both start up and operate efficiently at low input voltages is ideally suited for single-cell alkaline products.

The LTC®3526L is a 1MHz, 550mA synchronous step-up (boost) converter with a wide input voltage range of 0.7V to 5V and an output voltage range of 1.5V to 5.25V. Housed in a 2mm × 2mm DFN package, the LTC3526L has a typical startup voltage of just 700mV, with operation down to 400mV once started. Despite the LTC3526L's tiny solution size, it includes many advanced features, including output disconnect, short circuit protection, low noise fixed frequency operation, internal compensation, soft-start, thermal shutdown and Burst Mode® operation for high efficiency at light load. For low noise applications, the LTC®3526LB offers fixed frequency operation at all load currents. With an output voltage range that extends down to 1.5V, the LTC3526L and LTC3526LB can even be used in applications previously requiring a boost converter followed by a buck converter.

A typical single-cell boost application is shown in Figure 1. In this example the LTC3526LB is used to generate 1.8V for a Bluetooth radio application. The LTC3526LB was selected for its small size, minimal external component count and low-noise, fixed frequency operation at all load currents. A graph of output current capability versus input voltage is shown in Figure 2. Note that the converter starts up at 700mV at no load and once run-

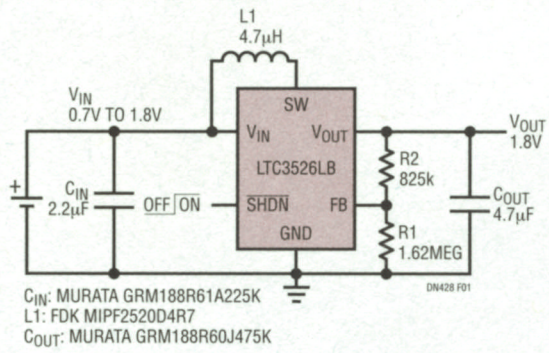

Figure 1. Single-Cell 1.8V Boost Converter for a Bluetooth Radio Application Features a Low Startup Voltage and Uses a Monolithic Chip Inductor for a Maximum Component Height of Just 1mm.

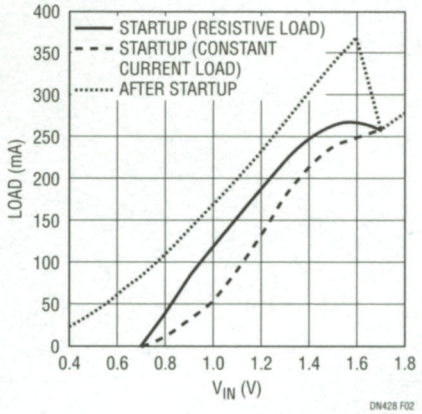

Figure 2. Maximum Load Capability During and After Startup for the Circuit in Figure 1.

ning, can deliver 25mA of output current with an input voltage of only 400mV. The 1MHz switching frequency allows the use of small, low profile inductors, such as the monolithic chip inductor shown in this application. This provides a complete solution with a footprint that's just 36mm^2 with a 1mm profile.

Many new battery types are available to the consumer, some of which are aimed at high-tech, high power applications. One of these is the disposable lithium AA/AAA battery, which offers a significant improvement in runtime over traditional alkaline batteries. Furthermore, in applications that see infrequent use, the long shelf life of lithium batteries gives them a performance edge over nickel-based rechargeable batteries, which have a high self-discharge rate.

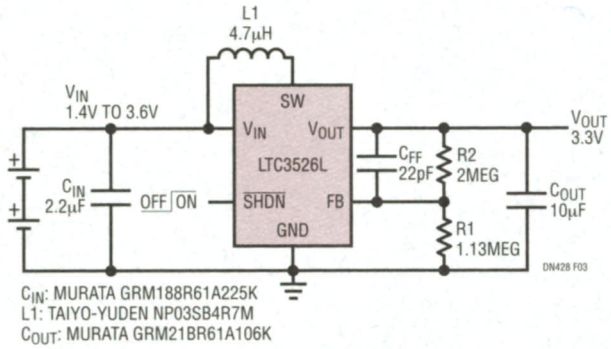

Figure 3. Two AA Lithium Cell to 3.3V Boost Converter with 250mA Load Capability Maintains High Efficiency Over Three Decades of Load Current and Operates with $V_{IN} \geq V_{OUT}$.

One characteristic of the lithium battery is that its voltage can be as high as 1.8V when the battery is fresh, compared to 1.6V for a typical alkaline battery. This is a problem for 2-cell alkaline applications that use a traditional boost converter to produce a 3.3V output from an alkaline 3.2V max input. Most boost converters cannot maintain regulation when the input is higher than the output, as it is with two fresh lithium batteries (3.6V).

The LTC3526L solves this problem by maintaining regulation even when the input voltage exceeds the output voltage. An example of a 2-cell to 3.3V boost converter using the LTC3526L is shown in Figure 3. A small feedforward capacitor has been added across the upper divider resistor to reduce output ripple in Burst Mode operation. Efficiency vs load curves are shown in Figure 4. These curves demonstrate the high efficiency at light load made possible by the low 9µA quiescent current of Burst Mode operation. The curve in Figure 5 illustrates the efficiency at input voltages above and below the output voltage.

Conclusion

The LTC3526L is a highly integrated step-up DC/DC converter in a 2mm × 2mm package designed to easily fit a wide variety of battery-powered applications. Low startup and operating voltages extend runtime in single-cell applications. It even regulates in step-down situations where the fresh battery voltage (V_{IN}) may exceed V_{OUT}. For high efficiency at light loads, or low noise operation, it offers a choice of Burst Mode or fixed frequency operation.

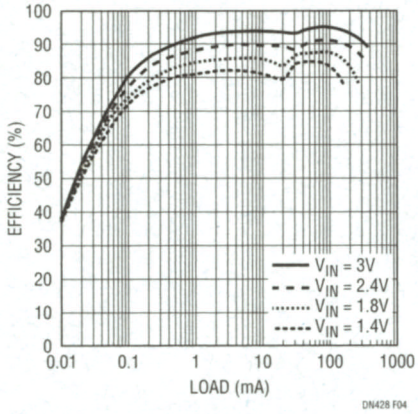

Figure 4. Efficiency vs Load for the Circuit in Figure 3.

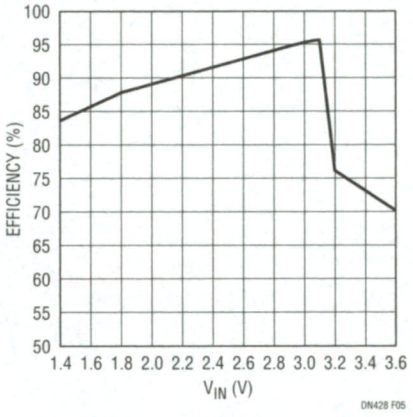

Figure 5. Efficiency vs V_{IN} for the Circuit in Figure 3 (at 100mA Load Current).

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Handheld oscilloscopes offer varied features

A HANDS-ON EVALUATION OF FOUR MODELS SHOWS A WIDE ARRAY OF PERFORMANCE, FEATURES, AND PRICE.

BY MARTIN ROWE • *TEST & MEASUREMENT WORLD*

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Engineers once thought of handheld oscilloscopes as the smaller cousins of bench models, but they now offer performance levels that rival those of their larger cousins. They also add battery-powered operation and portability that the bench instruments lacked. To find out how this class of instruments—which cover a wide price range—stack up, I evaluated the 100-MHz, four-channel, $5995 AEMC OX 7104-C; 200-MHz, two-channel, $2999 Fluke 199C; 40-MHz, two-channel, $1651 Agilent Technologies U1604A; and 60-MHz, two-channel, $1686 Protek 860F. Tektronix also offers a handheld oscilloscope, the THS730, but the company chose not to participate in the evaluation. For a signal source, I used a 20-MHz Agilent 33220A function generator.

All four models include built-in DMMs (digital multimeters), and all come with oscilloscope and DMM probes. All except the Fluke instrument include communications cables and software as standard features. They all provide measurements such as rms voltage, peak-to-peak voltage, and frequency. All include some form of spectral analysis, and all except the Protek model include a data recorder. The Agilent and Protek models are comparable in price, and their firmware and software led me to believe that they come from the same source. Thus, this article covers them together, pointing out similarities and differences.

With handheld oscilloscopes, the intangibles can matter more than they do for bench instruments. For example, battery life, the ability to change batteries in the field, and screen readability in daylight are factors irrelevant to bench oscilloscopes. The online version of this article, at www.edn.com/071108df2, contains a link to **Table 1**, which compares features, prices, and my likes and dislikes. You can also link to my blog at www.tmworld.com/b1, where you can read detailed evaluations of the instruments.

AEMC OX 7104-C

AEMC's Model OX 7104-C is the only four-channel handheld oscilloscope on the market. Its 12-bit resolution, 100-MHz bandwidth, and touchscreen display put it high on the performance list (**Figure 1**). To justify its

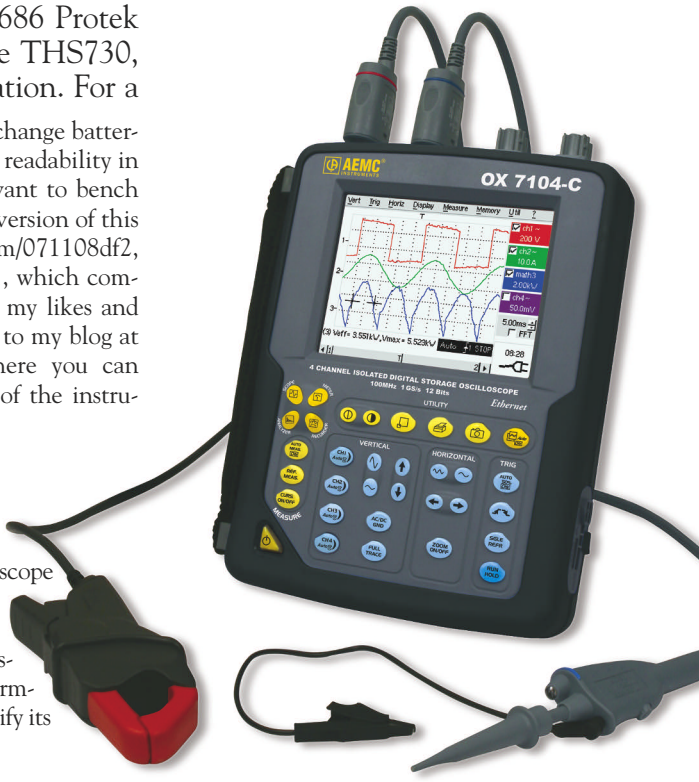

Figure 1 The AEMC OX 7104-C features a touchscreen at 12-bit resolution.

$5995 price, you'd better need the portability; AEMC offers a two-channel version for $3995. If you don't need the portability, you can find plenty of bench oscilloscopes with comparable performance and price, but most have 8-bit resolution as opposed to the AEMC unit's 12-bit resolution. The OX 7104-C's most striking physical features are its touchscreen and probes. The probes connect to the top of the scope through adapters permanently attached to the probe cables. The instrument knows whenever you connect a probe, and it detects the probe's attenuation level. The probes come with a handy light that you control with a button on the probe handle.

AEMC's ac-mains adapter is large, but the power supply is inline. Thus, its standard ac plug covers only one space on a power strip. The oscilloscope end of the power cord has a four-prong plug that looks as though it plugs in more than one way. Fortunately, it doesn't. You can also use separate adapters that provide BNC jacks for connecting cables. I used one to connect a function generator to the oscilloscope. Another adapter provides banana jacks for DMM probes. That feature is handy, because it lets you mix and match channels and thus connect oscilloscope probes; DMM leads; or accessories, such as current probes, to any channel. All other oscilloscopes in this evaluation have two oscilloscope channels and one DMM channel.

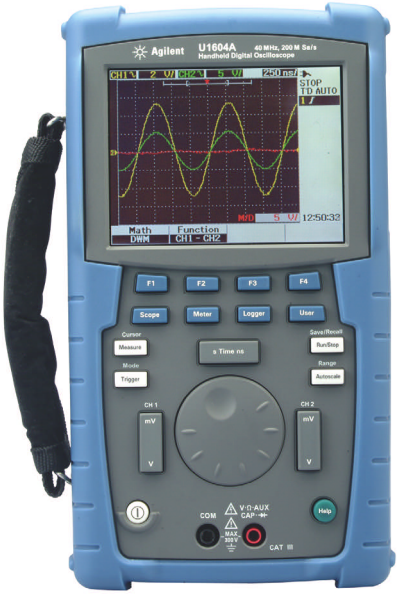

Figure 3 Agilent's U1604A provides both a wheel and buttons for setting the instrument.

AT A GLANCE

- Handheld oscilloscopes now offer performance levels rivaling those of bench models.
- The AEMC OX 7104-C's 12-bit resolution, 100-MHz bandwidth, and touchscreen display put it high on the performance list.
- Fluke's 199C ScopeMeter boasts the highest bandwidth of the lot—200 MHz—and the highest sampling rate: 2.5G samples/sec.
- Because the operations and prices of Agilent's U1604A and Protek's 860F are so similar, your choice comes down to small differences, such as PC connectivity, field-replaceable batteries, buttons, color displays, and handles.

The touchscreen lets you operate the instrument without using the buttons, although the buttons are neatly organized. If you use the stylus, you get more than one way to activate a feature. For example, you can change a channel's configuration by tapping on that channel's colored box on the screen or by using menus. The stylus attaches to the back of the case when not in use.

AEMC's handheld oscilloscope includes a harmonic analyzer for power-quality analysis and covers 40 to 450 Hz. At low-voltage levels, it provided reliable results to 5 kHz. I tested the analyzer with a sine wave and a square wave, seeing only the fundamental of a sine wave and only odd harmonics of the square wave, as I expected. The harmonic-analyzer display shows a signal's spectrum harmonics to the 30th harmonic with a check box under each one. Tapping the check box lets you display amplitude and phase information for that harmonic. The screen also displays rms amplitude and THD (total harmonic distortion) on the signal.

AEMC's SX-Metro software lets you import data from the OX 7104-C into a PC and remotely operate the oscilloscope in scope mode. I used the RS-232 connection first, and the PC quickly recognized the oscilloscope. Using it with the optional Ethernet link yielded different results, however. I had to go into the Options menu in the SX-Metro software to change the IP (Internet Protocol) address to match that of the scope. I kept getting a communication error on my PC, so I returned to RS-232 to evaluate the software.

Figure 2 Fluke's 199C ScopeMeter has the largest screen of the four oscilloscopes.

To send a screen image to the PC, you must use the oscilloscope's file manager. I found the file manager confusing to use and needed several tries to understand its operation. I also found the communication-cable connectors difficult to insert. You must press the connector's release button to insert it into the socket, and, even then, you must jiggle the connector to make a secure connection. You could break the clips if you push too hard. In addition, the molded cover designed for the communications and power connectors kept popping off, but the cover is attached to the unit, so you can't lose it.

The AEMC OX 7104-C is a powerful instrument. Its bandwidth and resolution make it a viable alternative to some bench scopes, and its ability to mix and match oscilloscope and DMM inputs with its four channels is unique. The instrument has a few quirks, though, particularly when saving files for PC downloading, and its price is difficult to justify.

FLUKE 199C SCOPEMETER

At half the price of the AEMC and nearly twice the price of the Agilent and Protek models, the Fluke 199C ScopeMeter boasts the highest bandwidth of the lot—200 MHz—and the highest

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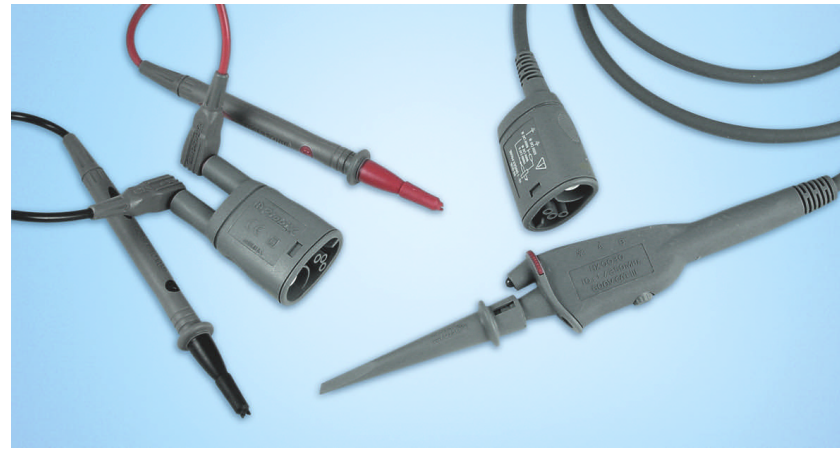
sampling rate: 2.5G samples/sec (**Figure 2**). Fluke pioneered the handheld-oscilloscope market, and the 199C has come a long way from the original ScopeMeter. The 199C is far easier to use than its ancestors. The buttons are neatly organized—though slightly too close together—and the four soft keys are easy to understand.

The screen is the largest of the four models I evaluated. It looks bright and clear when I used it indoors, but the plastic cover is so shiny that you can't see the traces outdoors because of reflections. The oscilloscope has a hand strap on its left side, but you can move it to the right side, making this the only one of the four instruments that addresses the needs of lefties. Moving the strap, however, means covering the optical communications port. The Fluke oscilloscope also has the most rugged stand of the group, and it is the only one with a strap that lets you hang the instrument while in use.

The ScopeMeter has two dedicated buttons, "Zoom" and "Replay." The zoom button cuts the time/division in half, which gives you a quick two-times zoom of the waveform. The replay button gives you a link to the past, letting you view the last 100 screens in reverse chronological order. When you exit the replay feature, you lose the data, because the scope starts recording the next 100 screens.

The Fluke recorder feature stands out. It has three modes, of which two are for the oscilloscope, not just for the DMM. The scope trend plot lets you record scope measurements such as peak-to-peak voltage, ac voltage, rise time, and frequency. I used it to record peak-to-peak voltage and frequency because they're easy to change in the function generator. The Scope Record option lets you store a long string of scope acquisitions into the unit's deep memory. The DMM recorder lets you plot a selected DMM measurement. I chose V rms and produced a trend plot.

Trend plots let you look at long-term changes in a signal. The 199C records data until its memory fills, and then it compresses the data to free half the memory and thus double the unit's capacity. Record size is 27,000 points per input. You can set the instrument to stop recording when the memory is full, and you can use the time/division button to increase or decrease the time/recorder screen.



Adapters for the AEMC oscilloscope let you mix and match scope and DMM channels.

The FlukeView software lets you take a snapshot of the instrument's screen, but it doesn't provide oscilloscope updates in real time. It also provides limited online control of the instrument—once you find that feature in the program's Instrument menu. You can change modes, including scope, meter, and logger, and you can recall setups. You can operate the recorder to capture DMM measurements in real time as well as save setups, print, and log data to the PC. You can also get a spectrum display of an input signal after first downloading a waveform display.

The Fluke 199C is a powerful handheld oscilloscope. If you're left-handed, it's the one for you. Its hanging strap makes the instrument useful for electrical applications in which you often need both hands free. The software is good for downloading data for offline storage and analysis. Perhaps the only drawback is the highly reflective screen cover.

AGILENT AND PROTEK UNITS

Because of the striking similarities between the Agilent and Protek instruments, you can't talk about one without talking about the other. So, I'll first discuss their similarities and then point out their differences.

The user interface on both instruments uses four soft keys and a wheel. I found Protek's wheel easy to spin, but Agilent's was difficult, often requiring two hands. The soft keys let you set parameters such as oscilloscope vertical and horizontal scales, triggers, measurement functions, math, and utilities. One utility lets you enable or disable the instrument's mini-USB connectivity port and the standard USB port for use with flash memory. You must navigate the utility menu to find the setting to enable the USB ports. With USB off, you get no communications or flash-memory access.

Measurement functions include peak to peak, rms, frequency, rise time, and fall time. You make a measurement by pressing the corresponding soft key and using the wheel to scroll through the choices. The math menu also lets you select FFT and a filtering window—

Figure 4 Protek's 860F would benefit from buttons for vertical and horizontal settings.

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- ✓ Integrate Traditional Power Management Solution ICs
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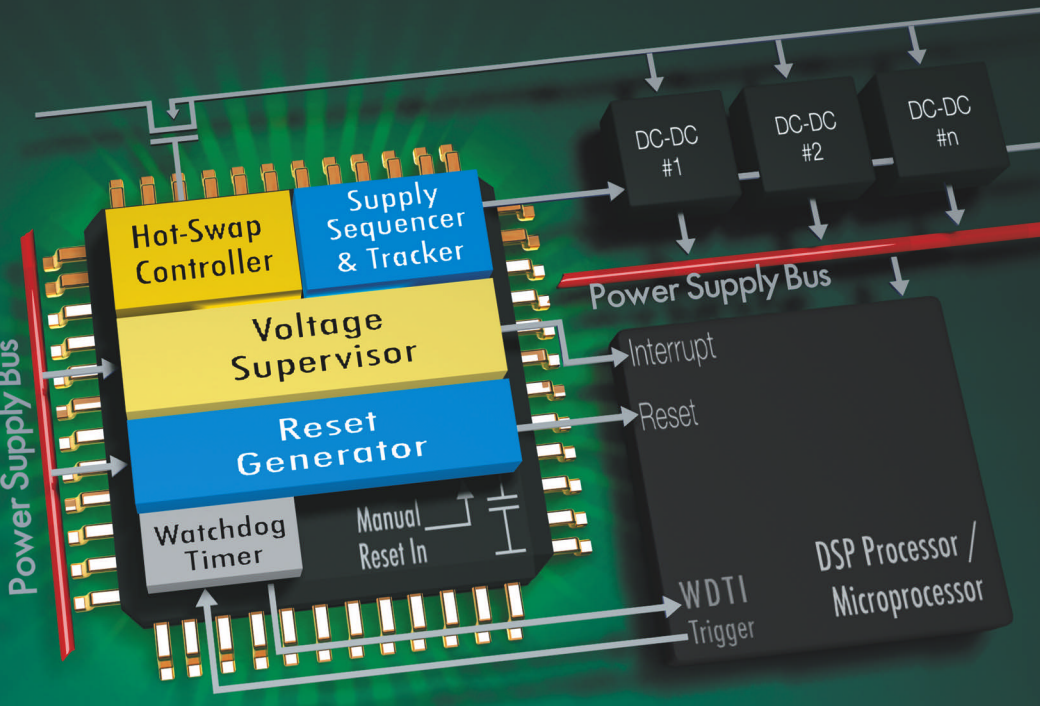

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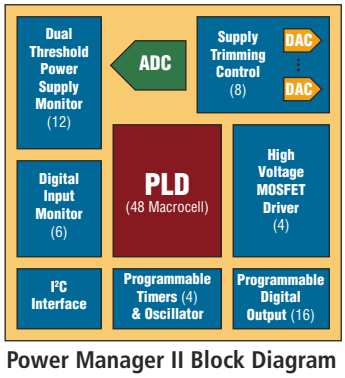
Power Manager II devices deliver a low-cost, easy-to-use solution for managing power and start-up functions. These mixed signal devices contain precision threshold comparators for monitoring power supplies, a 10-bit ADC for measuring power supply voltages, multiple DACs to control power supply output voltages, programmable logic to intelligently control power supply sequencing and generation of supervisory signals, programmable timers for controlling the speed of the power supply turn on/off process, charge pumped drivers for driving n-channel MOSFETs, digital inputs for controlling and monitoring system-level signals, and an I²C interface. With Power Manager II you simply get More of the Best.



Power Manager II Block Diagram

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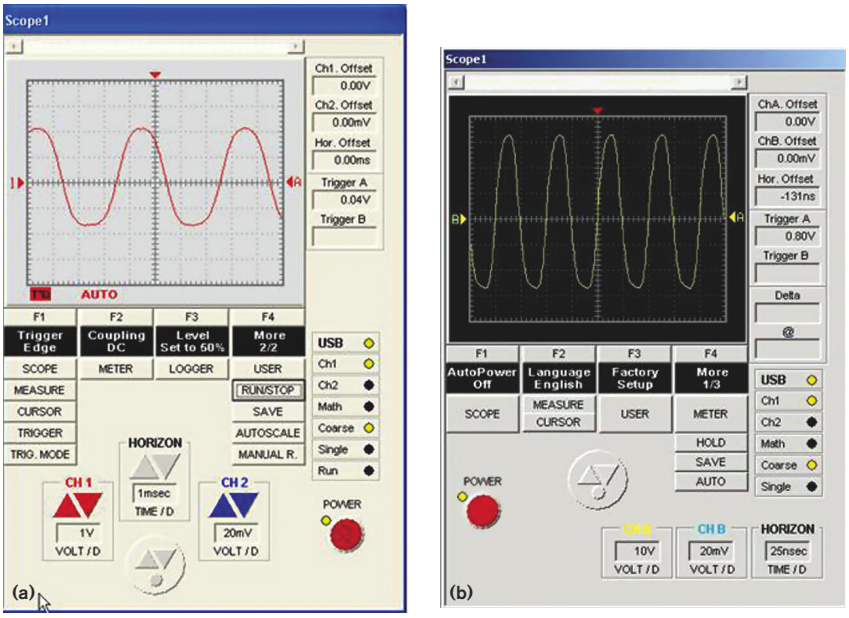

Agilent's PC software (a) and Protek's PC software (b) bear striking similarities, as do their firmware.

Hamming, Hanning, Blackman, or rectangular—and you can get spectral plots in real time on the screen.

Pressing the Meter button brings up a blank screen with three soft-key options: voltmeter, ohmmeter, and auxiliary meter. Pressing the auxiliary-meter key (F3) brings up choices for temperature, current, humidity, and pressure. For the voltmeter, you can choose from ac/dc, minimum/maximum, and relative measurements. To return to other meter functions, you must press the meter button, which brings you to the top of the meter menu; there's no "back" button. Pressing the ohmmeter button gives you resistance, diode, continuity, and capacitance measurements. (I wouldn't have expected to find capacitance buried under ohms, though.) You make your selection by repeatedly pressing the F1 key.

The only significant difference between the Agilent (**Figure 3**) and the Protek (**Figure 4**) user interfaces occurs on the screen when you enter DMM mode. The Agilent screen describes the meter functions, whereas the Protek screen is blank until soft-key functions appear.

Both instruments let you save screens and waveform data to a USB flash drive. You can save screens in graphical formats for importing into reports, and you can save data in text format for importing into Excel or other software. You can also save screens in a proprietary format that you can open with the PC software.

The PC software on the two instruments is also strikingly similar, right down to the word "horizon" over the horizontal scale (time/division) indicator. The software lets you take complete control of the instrument and get screen updates in real time. It also lets you view measurement parameters, save waveforms in digital form, and capture screens. Once you install the software and turn on each instrument's USB function, you establish communications by clicking on the virtual power button.

Hardware, firmware, and PC-software differences, however, are worth noting. Agilent provides buttons for vertical and horizontal screen settings. Protek makes you change all settings through menus. Agilent uses a color screen, whereas Protek's screen is monochrome, and the monochrome screen is easier to see in daylight than the color screens from Agilent, AEMC, and Fluke. Protek gives you 20 MHz more bandwidth than Agilent. Both companies offer 20- and 40-MHz models, with Protek also offering a 60-MHz model. Agilent includes a logger function for recording DMM measurements. Protek doesn't.

Other physical differences include a strap on the Agilent unit only. Both in-

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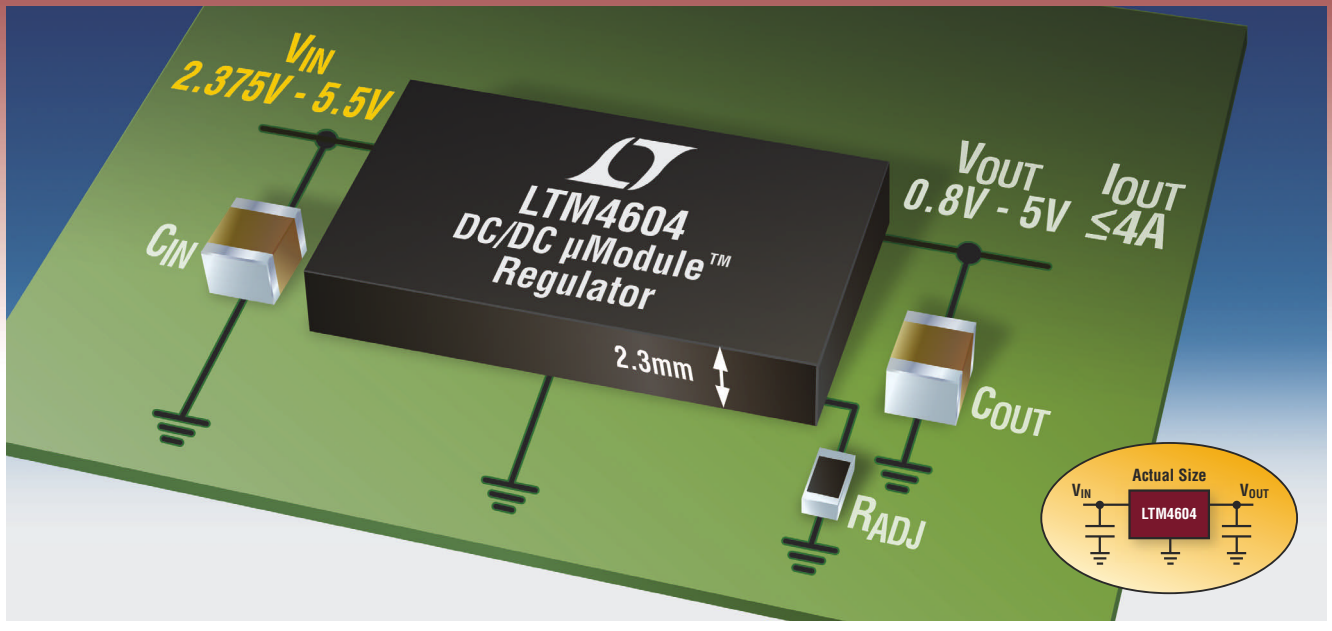
Low Profile, Low V_{IN} 4A DC/DC µModule



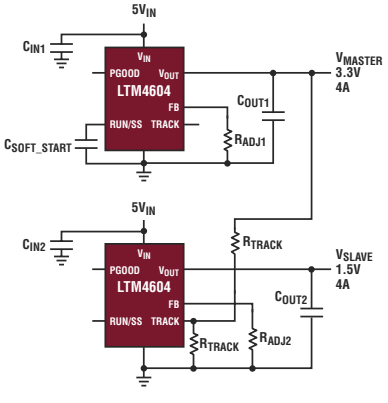
Thin, Simple & Complete DC/DC System

The LTM®4604 is a complete 4A, low voltage, switchmode DC/DC regulator system in a 9mm x 15mm LGA package with only a 2.3mm profile. Its encapsulated design improves system reliability while its low thermal impedance safely allows up to 12W to be delivered to a load. Furthermore, the LTM4604 provides output voltage tracking and IC-level quality and reliability in a tiny, low profile package.

Features

- Onboard Inductor, Power Components, DC/DC Regulator, Input/Output Bypass Capacitors
- 2.375V≤V_{IN}≤5.5V, 0.8V≤V_{OUT}≤5V
- 9mm x 15mm x 2.3mm LGA Package
- Current Mode Operation for Fast Short-Circuit Response, Accurate Current Limiting & Current Sharing
- Output Voltage Tracking
- ± 2% V_{OUT} Accuracy (-40°C to 85°C)

Simple, Dual 19.2W POL Solution



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struments have a holster, but Protek's is rather loose-fitting. Protek is the only oscilloscope of the four that lets you install any AA-size batteries, which means you can buy extra batteries anywhere. The others force you to buy a custom battery pack. Protek's stand design requires you to push and pull on it to lock it into place. I nearly broke the stand the first time I attempted to close it.

Although the oscilloscope BNC connectors are mounted on top of both instruments, Agilent's case causes the connectors to be recessed, making it difficult to connect and lock the probes unless you have especially small fingers.

Protek's power button gave me problems. It is somewhat sticky. I had to pull it out with my fingernails each time I turned the unit on or off. The first time I attempted to shut down the unit, the button stuck in the on position overnight and drained the battery.

Although the PC software (Agilent PC Link and Protek WaveLink) is nearly the same, the installation procedures differ. With Protek, you simply run the setup routine. The drivers and oscilloscope application will easily install.

GIVEN THAT THE OPERATIONS AND PRICES OF THE AGILENT U1604A AND PROTEK 860F ARE STRIKINGLY SIMILAR, THE CHOICE COMES DOWN TO THE SMALL DIFFERENCES.

Communication to the instrument was easy once I enabled the USB port.

Agilent requires you to install the drivers separately. I was at first unable to get the Agilent U1604A to communicate with the PC. I believe the cause was the Protek driver, which uses the same files as Agilent. Several phone calls and e-mails to Agilent technical support failed. The solution: Reformat the PC's hard drive to eliminate all Protek drivers. Even then, the Agilent installation was awkward. It's easy to make a mistake and have the PC fail to communicate with the oscilloscope.

Given that the operations and prices of the Agilent U1604A and Protek 860F are strikingly similar, the choice comes down to the small differences. If you need PC connectivity, go with the Protek instrument until Agilent updates its software-installation procedure. Agilent claims that it has addressed these issues since I posted my blog. You should also select Protek if you need to replace batteries in the field or if you need the additional 20-MHz bandwidth. If you insist on buttons for basic oscilloscope settings, a recorder function, a color display, or a handle, then choose the Agilent model. EDN

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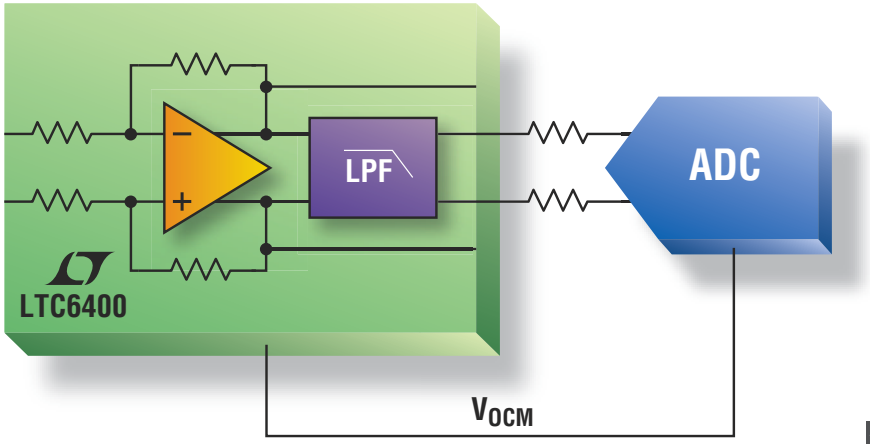
AUTHOR'S BIOGRAPHY

Martin Rowe is senior technical editor at Test & Measurement World *magazine* (www.tmworld.com), a sister publication to *EDN*.

2GHz ADC Driver

Get All the Bits You Paid for



Actual Driver Size
3mm x 3mm QFN

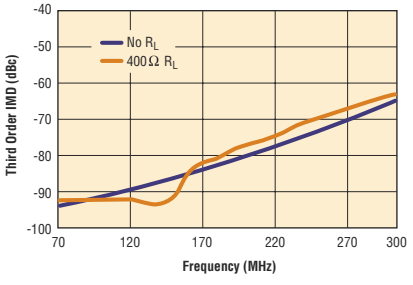
-93dBc IMD3 at 140MHz

Introducing the LTC®6400, an ADC driver with performance to match today's most advanced high-speed ADCs. Featuring excellent distortion performance and 1.8 nV/rtHz input-referred noise for 300MHz inputs, the LTC6400 is optimized for driving 12-bit, 14-bit and 16-bit ADCs. And it does this all on a single 3V supply at 270mW, while providing a differential output swing of $4.4V_{P-P}$. The LTC6400 fixed gain architecture eliminates several external components, simplifies design and maximizes performance.

Features

- 1.8GHz -3dB Bandwidth
- Fixed Gain of 10V/V (20dB)
- -93dBc IMD_3 at 140MHz
- 6.2dB Noise Figure
- 2.85V to 3.5V Supply Voltage
- 90mA Supply Current (270mW)
- Other Gain Options and Lower Power LTC6401 Also Available

Third Order Intermodulation Distortion vs Frequency
V_{OUT} = $2V_{pp}$ Composite



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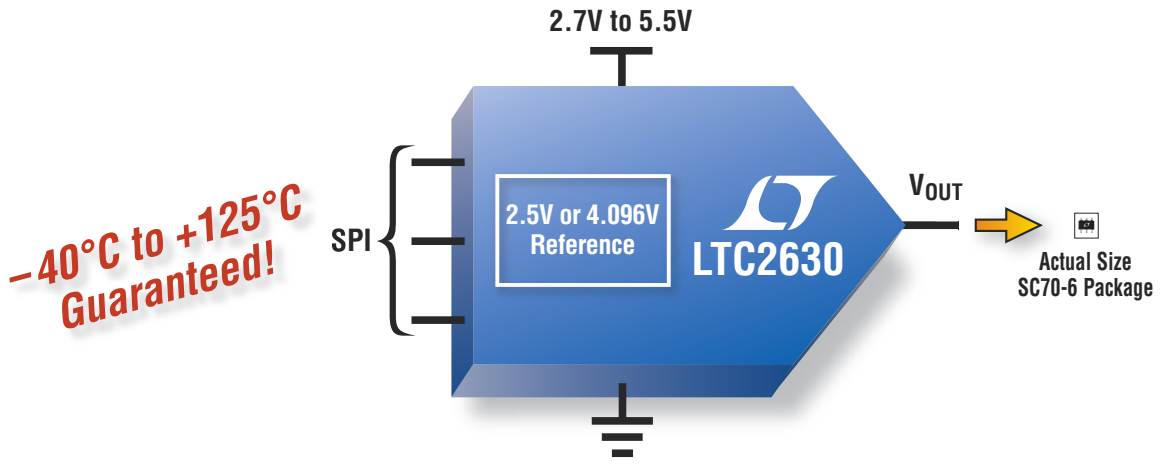
SC70 12-Bit DAC with Internal Reference



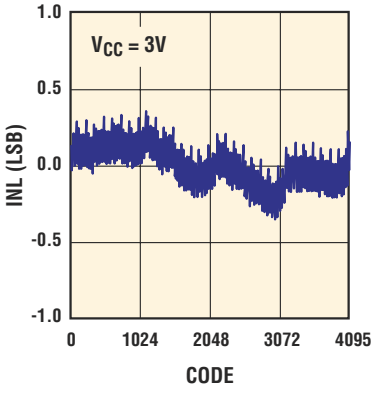
8-/10-/12-Bit DAC Family Guarantees ±1LSB INL from -40°C to +125°C

Packaged in the ultra-tiny 6-pin SC70, the LTC®2630 family of DACs includes an integrated reference and fits in half the space of competing solutions. These voltage output DACs offer the choice of an internal 2.5V or 4.096V reference and achieve ±1LSB INL at 12 bits of resolution. Ideal for control loop or trim applications, the LTC2630 family supports automotive temperatures and features pin- and software-compatibility.

Features

- Integrated Precision Reference:
  - 2.5V Full-Scale 10ppm/°C (LTC2630-L)
  - 4.096V Full-Scale 10ppm/°C (LTC2630-H)
- ±1LSB INL, ±1LSB DNL (LTC2630-12)
- Low Power: 0.54mW
- Pin-Compatible: 8-Bit, 10-Bit, 12-Bit Versions
- 6-Lead, 2.1mm x 2mm SC70 Package

LTC2630 12-Bit INL



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READERS SOLVE DESIGN PROBLEMS

Gain-of-two sample-and-hold amplifier uses no external resistors

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

When you need to simultaneously sample a signal and amplify the signal level, you can cascade a common gain-of-one sample-and-hold amplifier and an amplifier with a voltage gain of one. With some exceptions, such an amplifier has two external resistors (**Reference 1**). These resistors dissipate power even at the steady state of the sample-and-hold amplifier. In monolithic ICs, power dissipation and the consequent generation of heat from resistors are not the only items in the list of the drawbacks of external resistors. Integrating precise resistors within a silicon chip requires more processing steps, because such resistors are thin-film NiCr (nickel-chromium) or SiCr (silicon-chromium) elements. Manufacturers laser-trim these resistors to a tight tolerance value, contributing to the cost of an IC. Because these resistors occupy more chip area than standard signal-processing transistors,

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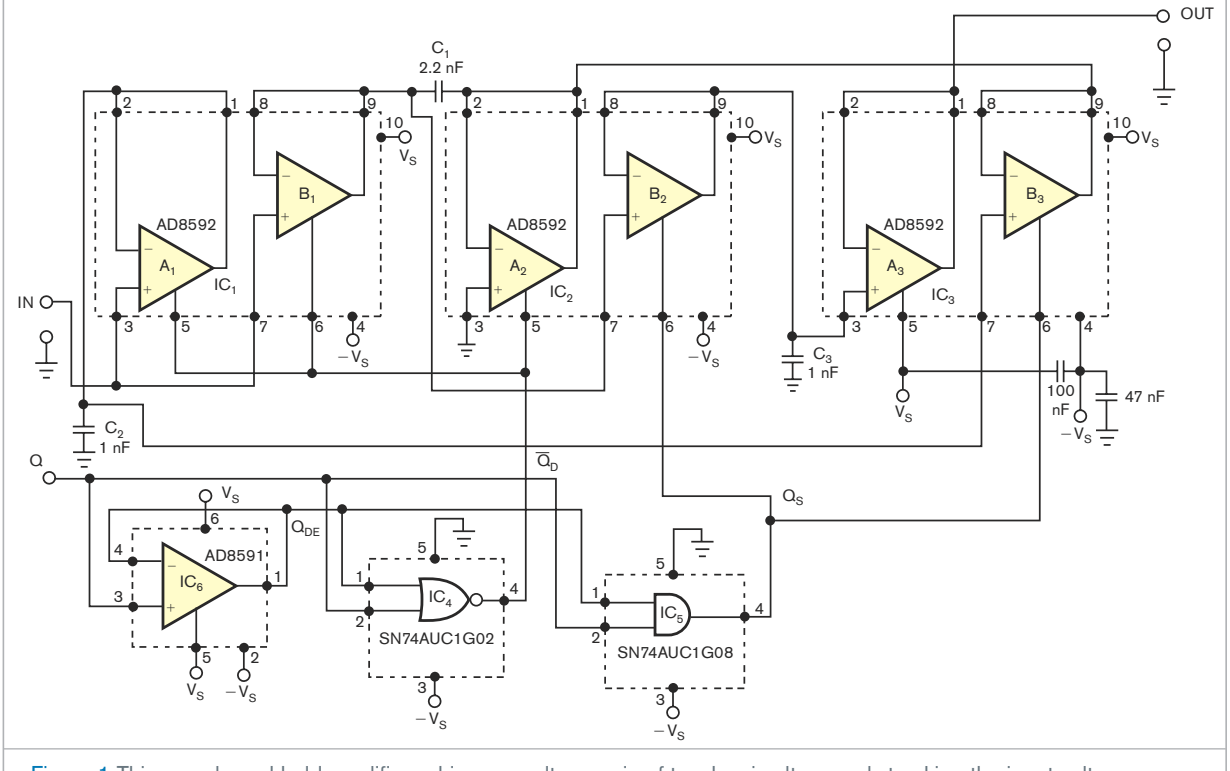

Figure 1 This sample-and-hold amplifier achieves a voltage gain of two by simultaneously tracking the input voltage on capacitors C_1 and C_2, "stacking" these capacitors within the sample interval, and storing the value of the stack's voltage in capacitor C_3.

the chip must be larger, further increasing the final cost. It's no wonder that designers of monolithic ICs as much as possible avoid using precision resistors.

If the required voltage-gain of a sample-and-hold amplifier is an integer, which it is in most cases, you can use an alternative way of increasing the magnitude of the output signal. For a voltage gain, G, the circuit can simultaneously track input voltage, V_{IN}, on temporarily ground-referenced tracking capacitors. Subsequently, an interruption occurs in tracking and cancels the ground referencing of G−1 of these capacitors. Meanwhile, the tracking capacitors stack on top of each other. The voltage on the stack is the sum of voltages of all of these capacitors, and it thus has the value of GV_{IN}. Upon the sample command, the constant voltage of GV_{IN} gets stored in the G+1 ground-referenced storing capacitor.

Figure 1 shows an example of a sample-and-hold amplifier with a voltage gain of two. Voltage followers control the potentials on capacitors C_1, C_2, and C_3 using their shutdown function. The design uses Analog Devices' (www.analog.com) AD8592 dual op amps because their output-leakage current in shutdown mode can be lower than 10 pA (**Reference 2**). You can follow the operation of the sample-and-hold amplifier with the timing diagram (**Figure 2**). The external logic-control signal, Q_S, is at a low level, and the C_1 and C_2 capacitors simultaneously track the voltage at its input. The shutdown inputs of followers A_1, B_1, and A_2 are tied together. At $\overline{Q}_D$=high, they are enabled, so the input voltage appears at the outputs of A_1 and B_1, and no voltage appears at the output of A_2. After the high-to-low transition of $\overline{Q}_D$, a dead slot follows with each of the controlled followers turning off. At Q=high, B_3 and B_2 turn on. Thus, the voltage in C_2 appears at the output of B_3. The potential of the input voltage occurs, therefore, at the lower node of C_1 (Pin 2 of IC_2). Because C_1's voltage has the same value as the input voltage and the output voltage, the B_2 follower is $2V_{IN}$. Capacitor C_3 thus charges to the voltage of $2V_{IN}$. After the high-to-low transition of Q_S, another dead slot follows to prevent any cross-conduction in the circuit. At the next high-to-low transition of Q_S, the process repeats.

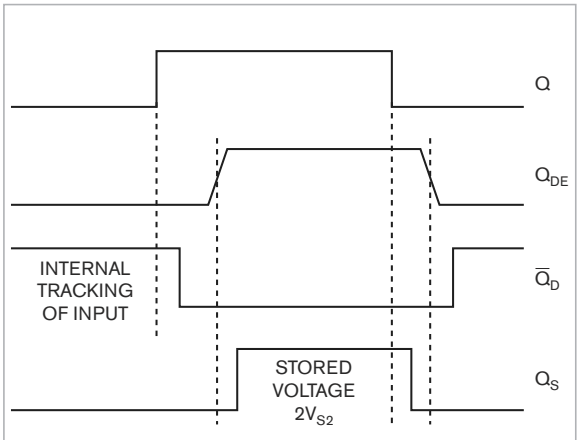

Figure 2 The external-control-logic signal, Q, splits into two quasicomplementary signals, Q_S and $\overline{Q}_D$, to avoid any internal cross-conduction in the amplifier.

The A_3 follower serves as an impedance converter, outputting the voltage in C_3. The single NOR and AND gates, together with op amp IC_6 functioning as a delay line, modify the single external-logic-control signal to create the properly timed internal logic signals, $\overline{Q}_D$ and Q_S.

For a noise analysis, assume that the noise characteristics of each of the followers are the same—namely, the standard deviation, σ_A, of the random component of the output voltage of a single follower. At the end of the tracking interval, both C_1 and C_2 charge to the input voltage. The standard deviation of the V_{C2} voltage is σ_A only for the A_1 follower. The standard deviation of V_{C1} voltage is, however, $\sqrt{2}\sigma_A$, because C_1 charges through two series-configured followers, B_1 and A_2. The standard deviation of $V_{C1}+V_{C2}$ voltage thus has the value of $\sqrt{3}\sigma_A$. The voltage of $V_{C1}+V_{C2}$ applies to C_3 through two followers in a cascade, B_3 and B_2, within the sample interval. Further, the V_{C3} voltage applies to the output through the A_3 follower. Because all of the noise sources are mutually independent and because they all effectively act in series, the standard deviation of the output voltage is $\sigma_{OUT}=\sqrt{6}\sigma_A$. Increasing the integer gain to the value of G yields $\sqrt{3G}\sigma_A$. You now pose an RSNR (relative signal-to-noise ratio) as gain, G, over a relative increment of noise at the output, yielding:

$$RSNR = \frac{G}{\frac{\sigma_{OUT}}{\sigma_A}} = \sqrt{\frac{G}{3}}.$$

For the sample-and-hold amplifier in **Figure 1**, the RSNR equals 0.8165, meaning that the noise characteristics of the circuit are slightly worse than those of a single follower. For a gain of three, the RSNR has the value of one, and, starting from a gain of four, at which the RSNR is 1.155, it gradually rises with increasing gain. The conclusion is that, for voltage gains of four or higher, the noise characteristics of the sample-and-hold amplifier are better than those of a single follower. EDN

IT'S NO WONDER THAT DESIGNERS OF MONOLITHIC ICs AS MUCH AS POSSIBLE AVOID USING PRECISION RESISTORS.

REFERENCES

1 Štofka Marián, "Gain-of-two instrumentation amplifier uses no external resistors," *EDN*, Feb 15, 2007, pg 81, www.edn.com/article/CA6413786.
2 "AD8592 Dual, CMOS Single Supply Rail-to-Rail Input/Output Operational Amplifier with ±250 mA Output Current and a Power-Saving Shutdown Mode," Analog Devices Inc, 1999, www.analog.com/zh/prod/0,,759_786_AD8592,00.html.

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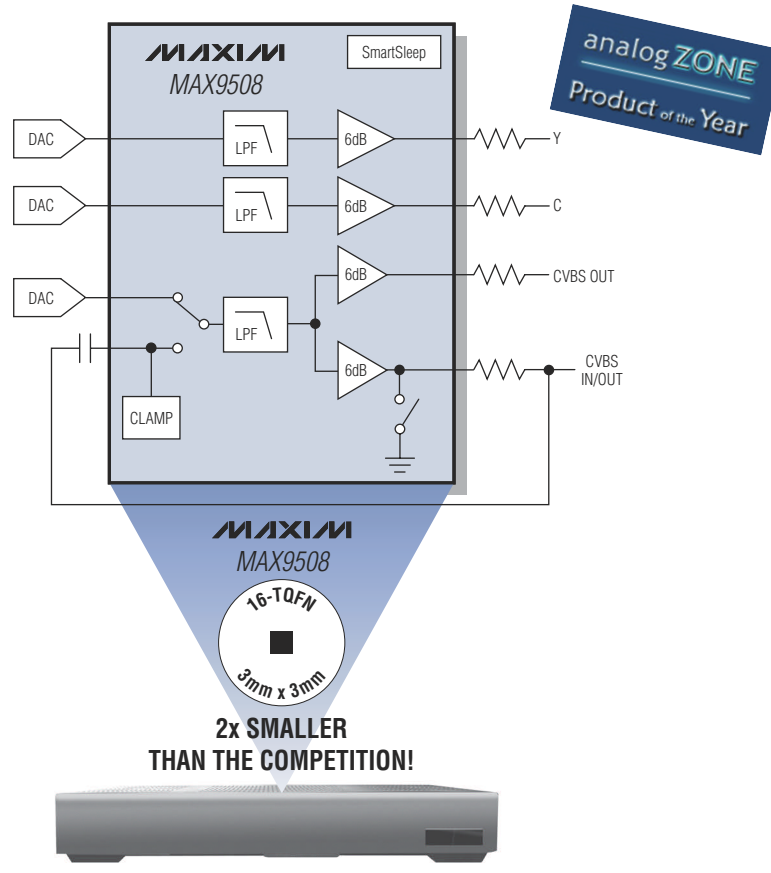

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Circuit for measuring motor speed uses low-cost components

R García-Gil, J Castelló, and JM Espí,
Escola Tècnica Superior d'Enginyeria, University of Valencia, Spain

This Design Idea uses a microcontroller, a 16×2-key LCD, and a rotary encoder to measure and visualize the speed of a motor (**Figure 1**). You measure the rotor speed of the motor using an incremental encoder coupled to the motor shaft, which provides quadrature pulses with a frequency proportional to the rotor speed. The 1024-pulse rotary encoder is the RS-32-0/1024ER.11KB from Hengstler (www.hengstler.com). You can calculate the rotational speed of the motor, ω_R, by counting the number of revolutions that the encoder axis, n_V, makes during a certain time period, t_P. You calculate n_V by counting the number of pulses, n_P, that the encoder generates during this fixed period, t_P: $n_V=n_P/1024$ for this encoder. And the rotational speed is

$$\omega_R = \frac{60\times n_V}{t_P} = \frac{60\times n_P}{t_P\times 1024} = \delta\times n_P,$$

where $\delta=60/(t_P\times 1024)$ rpm represents the resolution of the measured speed. To obtain a resolution of 1 rpm for this application, the fixed period you use as a timebase is 60/1024=58.59 msec. In this Design Idea, a low-cost microcontroller, the PIC16F873, IC_1, from Microchip (www.microchip.com) performs these operations. This microcontroller also drives the LCD, IC_2, which shows the rotational speed in rotations per minute.

In a similar fashion to the circuit in **Reference 1**, you apply the quadrature pulses of the encoder to IC_1's RB0/INT input, which generates a high-priority interrupt at the rising edge of the pulse. These interruptions allow you to compute n_P by increasing a counter, which initializes after it reaches fixed period t_P. Moreover, the microcontroller's internal 8-bit timer, Timer 0, registers t_P, which generates a t_M (timer interruption) each 286 µsec for a clock frequency, f_{CLK}, of 14.3 MHz: $t_M=4\times 2^8/f_{CLK}/4=286$ µsec. This calculation means that fixing the timebase, t_P, requires 205 timer interruptions (t_P/t_M).

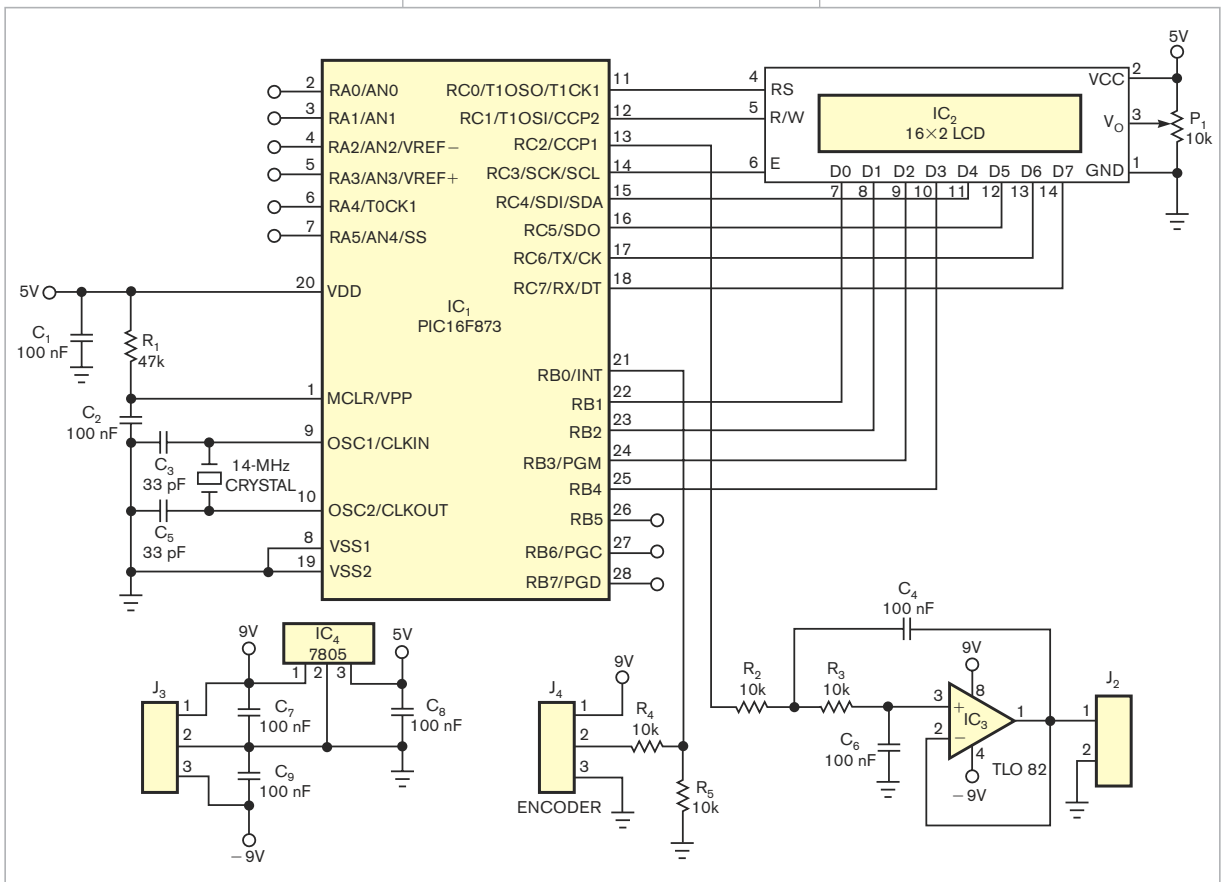

Figure 1 This circuit for measuring a motor's speed includes a PIC microcontroller and an LCD. It also provides an analog-to-digital conversion without an ADC.

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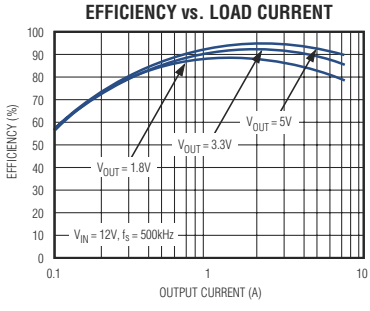

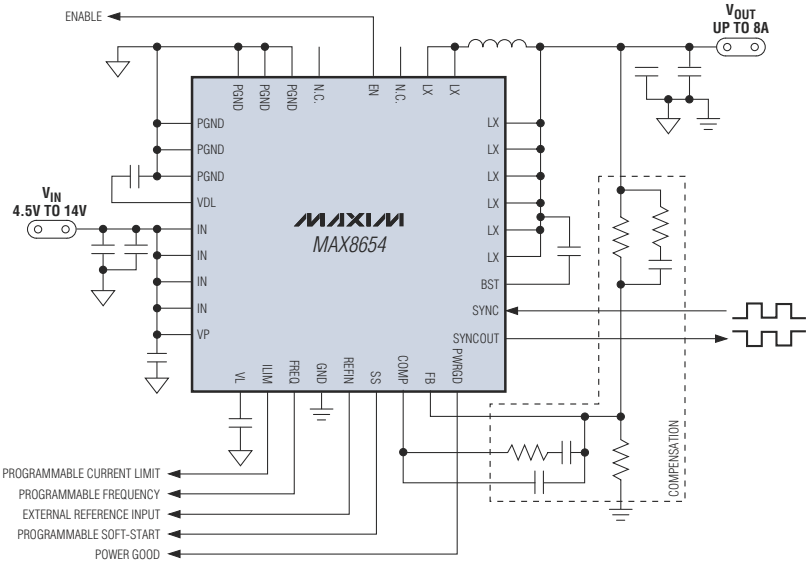

Features

- ♦ ±1% Output Accuracy
- ♦ 4.5V to 14V Input Supply
- ♦ 0.6V to (0.85 x V_{IN}) Adjustable Output
- ♦ 300kHz to 1MHz Adjustable Switching or SYNC Input
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- ♦ PGOOD and ENABLE for Sequencing
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When the counter reaches this time, the count, n_p, determines the rotational speed, according to the **equation**. Finally, this value appears on the screen of the LCD.

In addition, a digital-to-analog conversion is necessary if the control system must measure the rotational speed. You can do this conversion without adding an expensive DAC by applying a PWM (pulse-width-modulation) output of the microcontroller to a lowpass filter comprising R_2, R_3, C_4, C_6, and IC_3. The frequency of the PWM signal is 20 kHz, and the cutoff frequency of the lowpass filter is 160 Hz, which is much lower than the PWM frequency. In this design, the maximum duty cycle of the PWM signal corresponds to a rotational speed of 1500 rpm.

You can download the source code for IC_1's program from the online version of this Design Idea at www.edn.com/071108di1 and assemble the software with MPLab from www.microchip.com. You can alter constants within the software according to the encoder you use and your required resolution from the **equation**.EDN

REFERENCE

1 Jain, Abhishek, "Versatile digital speedometer uses few components," *EDN*, May 12, 2005, pg 95, www.edn.com/article/CA529384.

Battery monitor also enables constant-power-boost converter

Rex Niven, Forty Trout Electronics, Eltham, Victoria, Australia

Some microcontrollers permit operation below a supply voltage of 3V. This feature allows powering directly from a 3V alkaline or lithium battery without the voltage drop and leakage current of a regulator. It is important to monitor the battery voltage to ensure system integrity, and you can also use this information for system purposes. The circuit in this Design Idea maintains constant power to a white-LED-display backlight by adjusting the duty cycle of a boost-power converter. However, an ADC normally needs a fixed voltage reference (**Figure 1**), which would require two input pins for this function. This Design Idea turns the ADC's architecture inside out, providing the voltage-reference function using no extra pins.

The monitor circuit in **Figure 2** integrates an ADC within the microcontroller. The converter uses the battery voltage as a reference voltage. The principle is the opposite of normal: You want to measure a fixed voltage using a variable-voltage reference (the battery). For an 8-bit converter, the result for this example is $(1.18V/V_{BAT})\times256$. Note that a high value indicates that the battery voltage is low. Also, you can use the microcomputer pin that connects to the reference for another purpose. This example normally uses Pin 6 as an output to the pulse-indicator LED, LED_1. However, by briefly changing the port direction to analog-input mode, you can complete the battery-measurement operation, including settling, sampling, and conversion, in less than 0.1 msec.

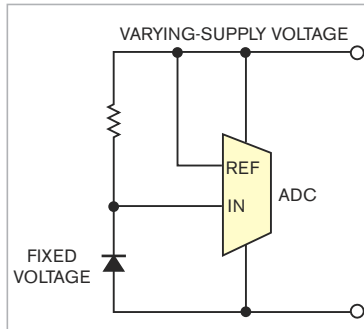

Figure 1 An ADC normally needs a fixed voltage reference, which would require two input pins for this function.

The example uses a PIC12F683 microcontroller and a voltage reference of 1.25V for the LM4041. R_1 biases the reference. R_2 ensures that the microcontroller output can rise to 3V to turn on transistor Q_1 without damag-

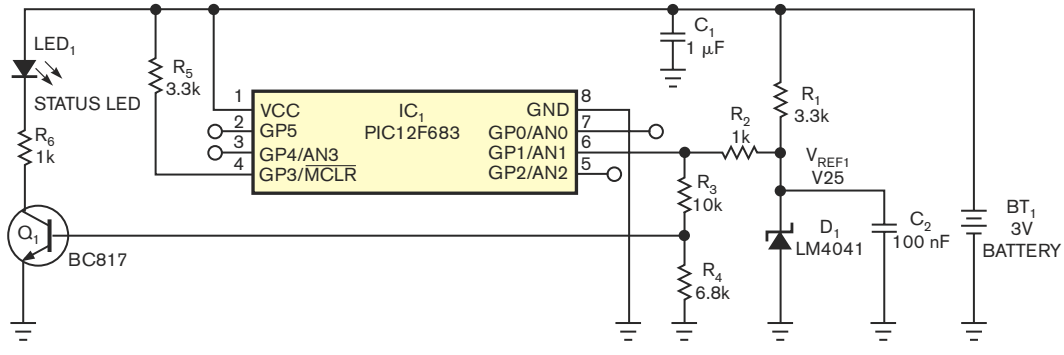

Figure 2 This monitor circuit integrates an ADC within the microcontroller. In this circuit, the converter uses the battery voltage as a reference voltage.

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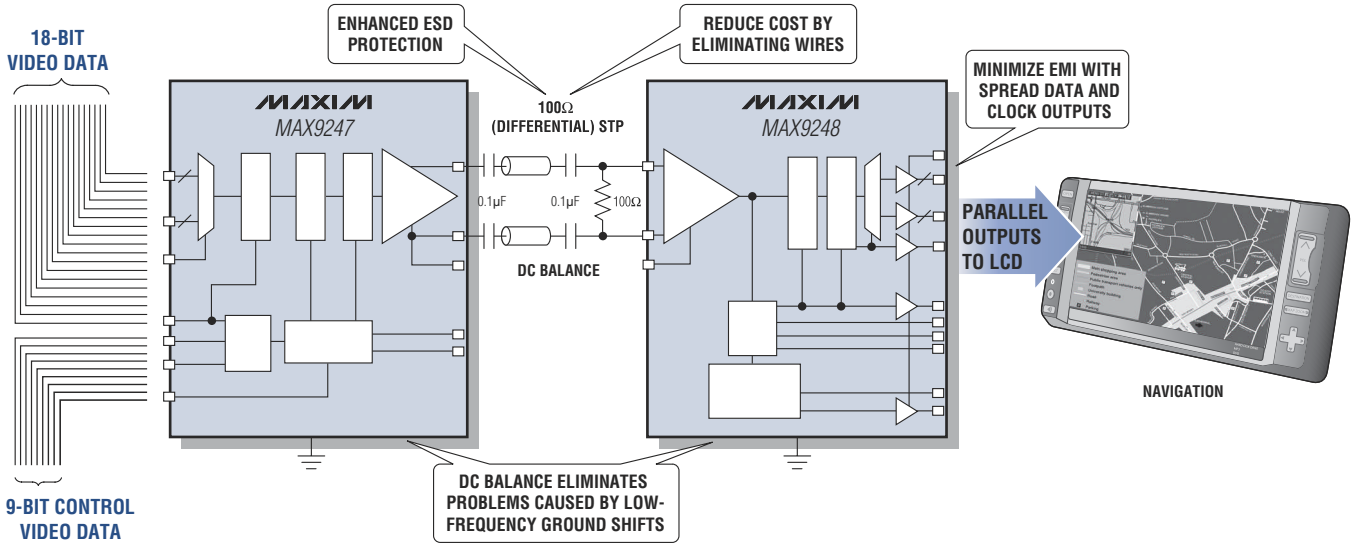

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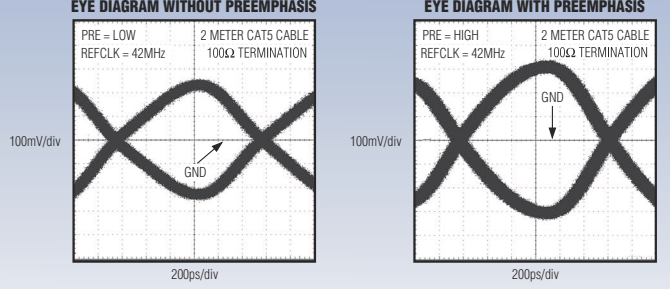
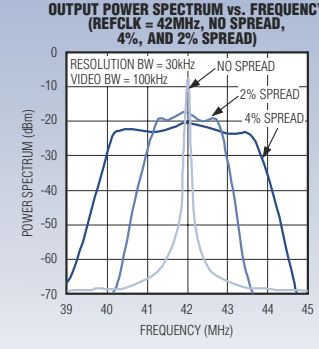


SPREAD SPECTRUM REDUCES EMI



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ing D_1. Resistors R_3 and R_4 ensure that the transistor is extinguished during the battery measurement. R_2, R_3, and R_4 introduce some attenuation, which you must take into account.

Figure 3 shows the monitor with the addition of a constant-power voltage-booster circuit. The PWM (pulse-width-modulation) output of the microcontroller drives the converter. For constant power from the booster, the required duty cycle linearly relates to the ADC's converted value.

Battery technologies vary in their discharge characteristics. Alkaline batteries have high capacity but drop their open-circuit voltage as they operate. The open-circuit voltage can provide a good estimate of battery charge. However, alkaline batteries also have internal resistance and exhibit a recovery phase after supplying a heavy load. The resistance increases with low temperature and low battery charge. To determine the battery's state, you can take measurements before and immediately after a high-current load is active. This approach allows estimation of both internal resistance and battery charge. EDN

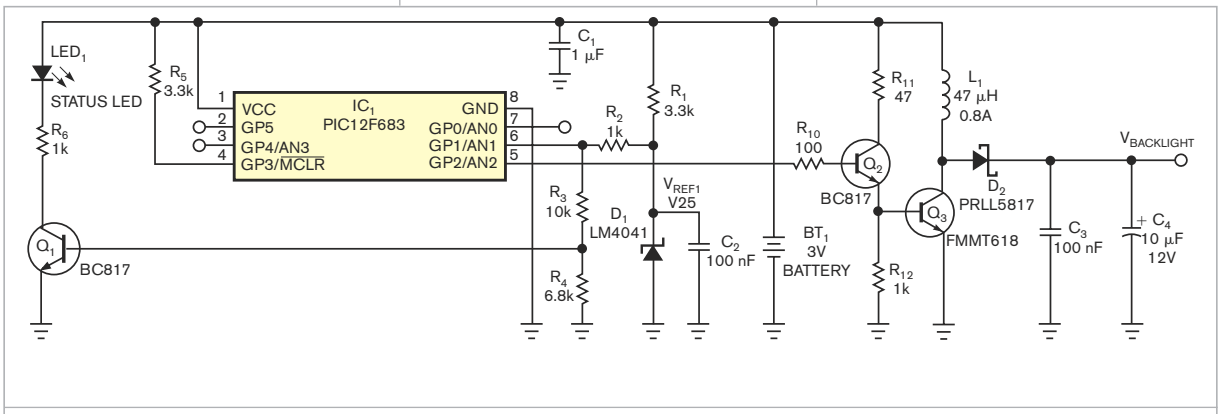

Figure 3 This monitor adds a constant-power voltage-booster circuit. The PWM output of the microcontroller drives the converter.

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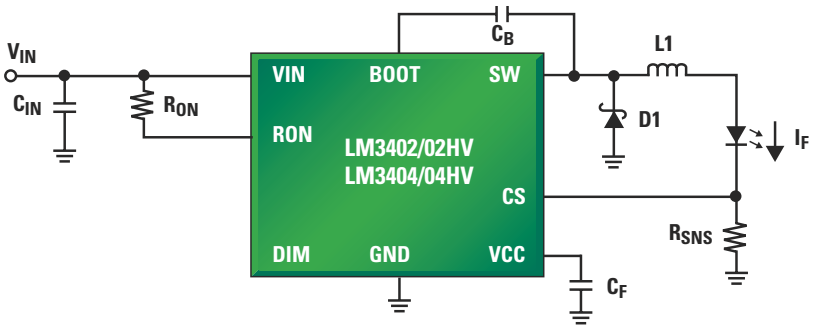
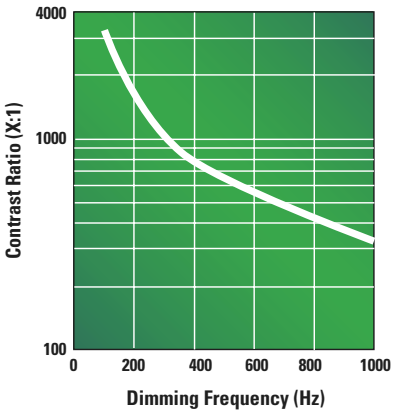


3000:1 Contrast Ratio when Dimming at 100 Hz



Buck LED Drivers

Product ID	Input Voltage Range (V)	Output Voltage (V)	Total LED Current (mA)	Number of LEDs in Series	Switching Frequency (kHz)	PWM Dimming	Key Features	Packaging
LM3401	4.5 to 35	0.2 to V_{IN} x 0.95	Controller	1 to 8	Adjustable up to 1.5 MHz	Yes	Hysteretic control yields extremely fast PWM dimming response. Adjustable hysteresis controls fsw or current ripple	MSOP-8
LM3402 **LM3402HV**	6 to 42 6 to 75	0.2 to V_{IN} x 0.9	500	1 to 9 1 to 15	Adjustable up to 1 MHz	Yes	Constant on-time yields fast PWM dimming response with controlled switching frequency	MSOP-8, PSOP-8
LM3404 **LM3404HV**	6 to 42 6 to 75	0.2 to V_{IN} x 0.9	1000	1 to 9 1 to 15	Adjustable up to 1 MHz	Yes	Constant on-time yields fast PWM dimming response with controlled switching frequency	SOIC-8, PSOP-8
LM3405	3 to 15	0.2 to 13.5	1000	1 to 3	1600	Yes	Internally compensated current-mode control	TSOT-6

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The Sight & Sound of Information

Arrow targets nontypical distribution with foundry play

The NAC (North American Components) business of Arrow Electronics Inc (www.arrow.com) is looking at distribution from a different angle. The Melville, NY, company recently established a relationship with IBM Global Engineering Solutions (www.ibm.com/technology). The relationship couples Arrow's custom-chip-design and -logistics capabilities with IBM's foundry products and services. The relationship targets the FPGA market, rather than the ASIC market, in which IBM has ties to top distributor and Arrow's chief competitor, Avnet Inc (www.avnet.com). With the addition of IBM-foundry services, Arrow believes it will be able to expand its custom-logic portfolio to reach a broader customer base.

"We're putting together long-term plans for a successful engagement that are from design services/COTS [commercial off the shelf], down to wafer," says Christopher Miller, director of Arrow's Custom Logic Solutions group. "It's a nontypical distribution agreement [compared with] what you've seen in history. We believe it's a first."

The move away from the traditional distributor-ASIC model was intentional, says Miller, who believes another ASIC relationship would not be the right economic model for the next few years and who maintains that customers want lower cost to entry for more complex products. "Foundry is different from ASIC. If you look at IBM and its substantial relationship with Avnet through the years, this [relationship] is a complementary model to an ASIC flow through Avnet. We believe that we bring a lot to IBM and that they bring a lot to us without upsetting IBM's current channel partners. Customers want to be able to make decisions based on what they have in the flexibility of their vendors, and we feel that we finally have that flexibility," he says.

GREEN UPDATE

UNITED KINGDOM WANTS TO KNOW WHAT YOU THINK OF ROHS

The United Kingdom is currently seeking opinions of electrical- and electronic-equipment producers about EU (European Union) ROHS (restriction-of-hazardous-substances) regulations, exempt applications, and enforcement in the EU member states. In doing so, the UK Department for BERR (Business, Enterprise and Regulatory Reform, www.berr.gov.uk) in September issued the "Consultation on the Changes to the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Regulations SI 2006/1463" document. The consultation seeks views on the proposed replacement of this document with a new set of ROHS regulations.

The consultation document does not seek views on the provisions of the directive itself, which the EU—not member states—governs, but on proposed changes to ROHS regulations that include "the way in which the regulations refer to those applications of hazardous substances that are exempt from the ROHS directive, and the provisions dealing with the investigation and enforcement of compliance with producers' obligations." BERR has set a closing date of Nov 29, 2007.

To respond to the inquiry, visit www.berr.gov.uk/files/file41224.pdf.

OUTLOOK

CONSUMER-ELECTRONICS DEMAND HIGH FOR THE HOLIDAYS

Demand for consumer electronics will once again be high this holiday season, with market-research company In-Stat (www.in-stat.com) reporting that more than 80% of respondents to a recent survey plan to purchase a consumer-electronics product during this holiday season. "In 2007, HDTVs [high-definition televisions] top consumers' holiday wish lists, most likely due to plummeting prices for these products," says Stephanie Ethier, an analyst at the company.

However, HDTV purchases won't be only for gift-giving. In-Stat reports that, although consumers will likely purchase portable products as gifts, they will likely purchase higher priced products requiring more research and preference, such as HDTVs and digital camcorders, for personal use.

Either way, In-Stat expects HDTVs to bump digital cameras, a long-time holiday-season top electronics choice, down to the third spot. In-Stat predicts that PCs will jump up to the second spot this year, as both desktop and laptop PCs advance into multimedia devices used for video viewing, music playback, and imaging applications. The company's survey received more than 2000 responses from North American consumers.

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Targeting ac-motor-drive applications, the symmetrical VFD (varying-frequency-drive) cables carry power from industrial ac-drive systems to ac motors. A dual-copper-tape shielding provides a low-resistance path to ground for improving common-mode-current containment. The dual spirally applied tapes allow improved flexibility and effective radiated- and conducted-noise protection. The cable reduces ac-motor shaft voltage by using three symmetrical bar-ground wires, providing a balanced ground system, and reduces the chance of premature motor-bearing or motor-insulation failure. Prices for the VFD cables range from $1.94 to $17.42/ft.
Belden, www.belden.com

SMT contacts come in a variety of heights and pitches

Providing an electrical connection between a device and a PCB (printed-circuit board), these single-piece, stamped SMT (surface-mount-technology) contacts use preload and antilift features. The contacts reduce qualification time by connecting a number of device components in any direction and configuration using the same interface. The universal contacts come in 1.3-mm heights with a 1.35-mm pitch, 1.8-mm heights with a 1.25-mm pitch, 2.5-mm heights with a 1.35-mm pitch, and 3.5- and 4-mm heights with a 1.45-mm pitch. Side wings protect the active parts of the contact, preventing contact from overstressing and potential damage, and a solder well prevents solder from wicking up the contact. Prices for the SMT contacts range from 5 to 8 cents, depending on volume.
ITT Electronic Components, www.ittcannon.com

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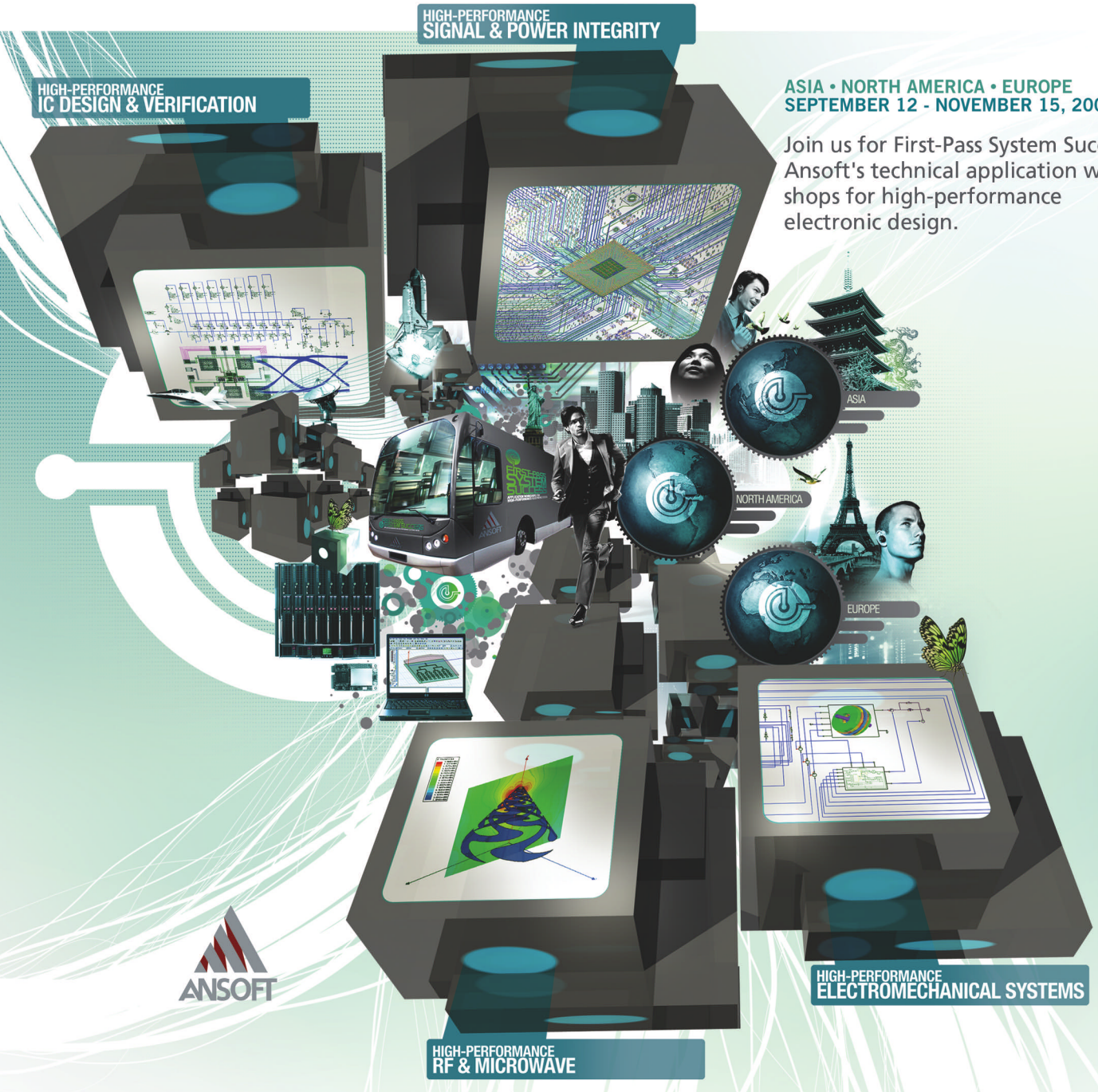

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definition-multimedia-interface) interconnect series with a thin, flexible, and durable cable. The interconnects come in 50 and 100m lengths, provide 1080p HD resolution over long distances, and are dimensionally HDMI-compliant from end to end with no bulges in the cable or bulky connector heads. The 50m version costs $1499, and the 100m version costs $2299.
VizionWare, www.vizionware.com

ZIF connector series comes in upper- and lower-side-contact versions

Targeting mobile phones, digital still cameras, digital videocameras, and display applications, the YLL ZIF (zero-insertion-force) connector series comes in a D-Series and a U-Series. The D-Series has bottom-side contacts, and the U-Series features upper-side contacts. Both series include 0.3-mm spacing and 13 to 45 contact positions. The D-Series has a 1-mm maximum height; the U-Series has a 1.05-mm maximum height. Available in a 0.3-mm pitch, the 41-position ZIF connector costs 57 cents for one to 5000 units.
FCI, www.fciconnect.com

Two-conductor connector splices three- and five-conductor connectors

Adding to the vendor's Lever-Nuts 222 compact-connector series, the 222-412 connector has a two-conductor splice joining the three- and five-conductor models in the series. The device has a UL/CNL listing as high as 600V/20A and accommodates solid and stranded conductors in sizes ranging from AWG (American wire gauge) #12 to 28 in the same unit. The Lever-Nuts 222-412 costs $19.50 (100).

Wago Corp, www.wago.com

COMPUTERS AND PERIPHERALS

Monitor has high NTSC color gamut

Featuring nearly 100° of NTSC color gamut for CCFL (cold-cathode-fluorescent-lamp) displays, the 19-in. SyncMaster has a 2000-to-1 contrast ratio. The TFT (thin-film-transistor) LCD monitor also offers a 2-µsec response time. The SyncMaster 931C costs $299.99.
Samsung, www.samsung.com

DVD-RAM drive features a high-speed USB interface

Measuring 5.43×6.38×0.87 in. and weighing less than 1 lb, the PX-608U portable DVD±R/RW CD-R/RW drive has a 2-Mbyte buffer and buffer-underrun-proof technology. The device supports 5× DVD-RAM and offers as much as 9.4 Gbytes of storage per double-sided disc. The device also has recording speeds of 8× DVD±R on single-layer media and 4× DVD±R on dual-layer media. The drives support 8× DVD+RW, 6× DVD+RW, 8× maximum DVD-ROM, and 24× CD-R/RW/ROM. The PX-608U costs $199.99.
Plextor, www.plextor.com

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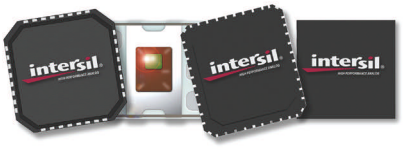

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X1950 CrossFire Edition graphics cards employ GDDR4 (series four of graphics-double-density-rate) memory technology. The X1950 series cards each cost $449.

ATI Technologies, www.ati.com

Controllers, adapter connect devices to desktop

The IDE JBOD (just-a-bunch-of-disks)/RAID (redundant-array-of-inexpensive-disks) PCIe (PCI Express) controller adds an extra channel, RAID capability, and JBOD capability to any desktop system, and you can install it in the PCIe slot of either a standard-height or a low-profile PC. The firmware enables setup of the two hard drives as RAID 1 for real-time backup, as RAID 0 for high performance, or as JBOD to combine the capacity of the two hard drives into one large volume. The USB 2.0-to-eSATA (external-serial-advanced-technology-attachment) adapter is compatible with port multipliers. The PCIe ExpressCard controller provides a way to add an ExpressCard socket to any desktop. The IDE JBOD/RAID PCIe controller and the USB 2.0-to-eSATA adapter cost $29.95 each. The PCIe ExpressCard controller costs $32.95.

Addonics Technologies, www.addonics.com

1-Tbyte external-storage system has two RAID options

Shipped in the RAID (redundant-array-of-inexpensive-disks) 0 setting, the user-serviceable My Book Pro Edition II consumes less than 26 in.^{2} of desk space and includes EMC Retrospect Express Version 7.5 backup and system-recovery software. Users can set the device to reserve half of its capacity to mirror users' data in real time using the RAID 1 setting. The device also has FireWire 800, FireWire 400, and USB 2.0 interfaces. The My Book Pro Edition II costs $549.

Western Digital Corp, www.westerndigital.com

High-performance monitors feature high contrast ratio

The 17-in. SyncMaster 731BF and 19-in. 931BF monitors feature a 2000-to-1 dynamic-contrast ratio with a 2-μsec response time. The 19-in. 971P features a 1500-to-1 contrast ratio, a 6-μsec response time, a 178/178° viewing angle, and a 1280×1024-pixel resolution. The SyncMaster 971P, 731BF, and 931BF cost $379.99, $249.99, and $299.99, respectively.

Samsung, www.samsung.com

Monitor integrates down-firing speakers

Offering a 5-msec response time, the LCD195WVXM monitor features a 1440×900-pixel native resolution and comes in a black cabinet. The LCD195WVXM monitor costs $284.99.

NEC Display Solutions, www.necdisplay.com

Hard drive comes with Retrospect Express software

Packaged with an eSATA (external-serial-advanced-technology-attachment) PCI card and cable, the 320-Gbyte eSATA/USB also comes with a USB 2.0 cable, a power cable, a quick-start guide, and a CD. The 320-Gbyte eSATA/USB costs $239.95.

Iomega Corp, www.iomega.com

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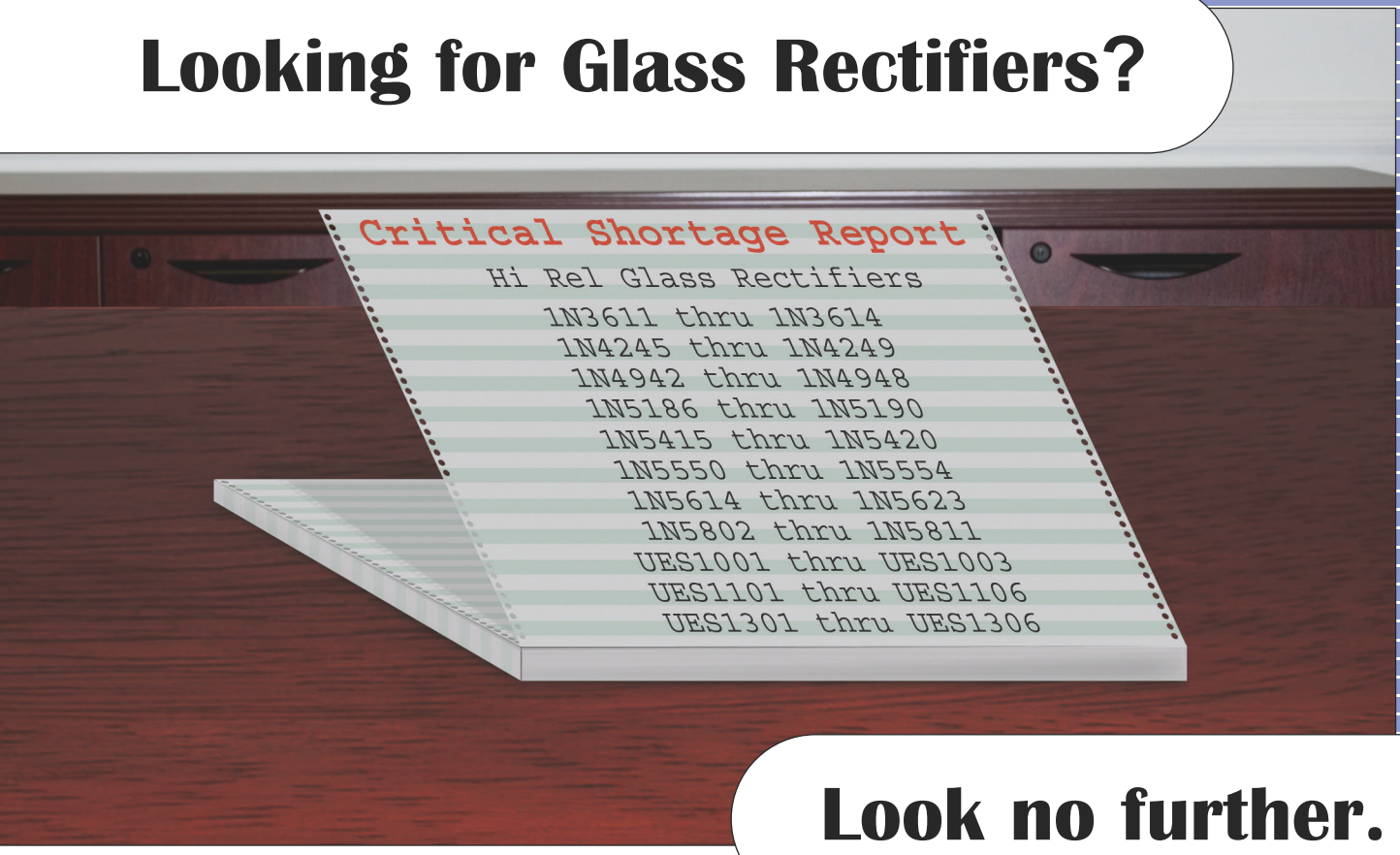

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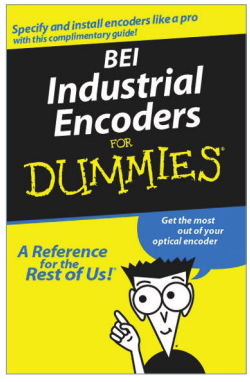

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scope

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LOOKING AHEAD

TO THE ELECTRONICS PACKAGING TECHNOLOGY CONFERENCE

Nobody should be in the dark at this point about the growing role of packaging technology in electronics design. It's not just about spreading heat and protecting the chip any more, and a quick review of subjects at this ninth Electronics Packaging Technology Conference (www.eptc-ieee.net/), December 10 to 12, should make that point clear. Keynotes will include Ralf Plieninger, senior director at Infineon, on packaging trends for mobile and communications platforms, and Herbert Reichl, a director at the Fraunhofer Institutes, on technologies for heterogeneous integration. Following that theme, invited papers will cover a range of packaging and technology issues, including mechanical reliability in package-on-package technology and the growing problem of whiskers in lead-free flip-chip packages. This conference is vital to engineers responsible for high levels of integration, and the Singapore location should provide a nice break from the December weather in the north.

LOOKING BACK

AT CONTINUING EDUCATION, 1950s-STYLE

The other night, I saw an auditorium of 750 seats filled to capacity—and then some—with Chicago-area engineers listening to the first of a series of eight lectures on transistors. This IRE-sponsored series brings engineers up to date on the present status and application of an important new component. Here is a practical solution to a problem every engineer faces: how to master new techniques. For eight weeks, these men will gather in this auditorium to hear lectures by engineers who do transistor design every day. The cost for the entire series, including a booklet and two-hour lecture followed by Q&A each week, is $6. An interesting sidelight is on-the-spot tape recording of the speaker's voice as he delivers the lecture. Recordings and illustrations will subsequently be available to groups or individuals at low cost.

—*Electrical Design News*, October 1957

LOOKING AROUND

AT THE GROWING ROLE OF GRAPHICS CHIPS IN SUPERCOMPUTING

When a component becomes cheap, people find novel ways of using it. This situation is certainly going on with the GPUs (graphics-processing units) that high-end game consoles and PC graphics cards use. Aside from being great graphics engines, the chips include large arrays of relatively capable integer ALUs, programmable and just waiting for repurposing. And new uses are appearing rapidly. GPUs have popped up in financial analysis, geological data reduction, and, in a nice irony, acceleration of the EDA codes necessary to design GPUs. It seems just a matter of time until the parts find their way into embedded-computing applications that could benefit from a thorough rethinking along the lines of "What if I had a free supercomputer array in here?"

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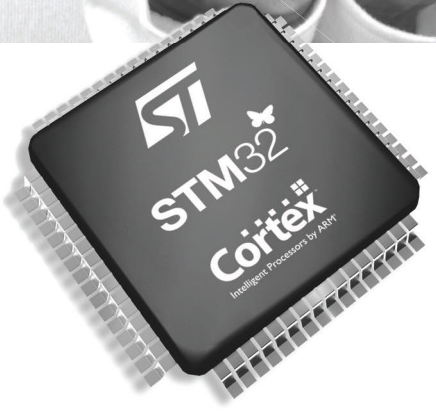

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